In Chapter 3, basic ESD protection mechanisms and device physics were discussed for single-element ESD protection structures, which are the foundation of all on-chip ESD protection design. These single-device structures have been dominating ESD protection solutions until early 1990s. However, modern ESD protection design is no longer a "device design" task. In addition, the old style of "one ESD protection structure for a chip" ESD protection design strategy does not hold any more in today's IC design. Advances in IC technologies make more robust but complex ESD protection circuits become attractive and feasible. Because of the facts that demands for ESD protection robustness increase continuously, complexity of IC functions requires customized ESD protection even within the same chip, and interactions between ESD protection structures and the circuit being protected become more and more important, development of advanced ESD protection solutions becomes a complex and challenging task that demands chip level consideration using a system approach. In this chapter, circuit level ESD protection solutions are discussed in great details.

4.1. INPUT ESD PROTECTION SCHEMES

Although many ESD protection structures can be used universally for input, output, power supply, and any other pads, design customisation is often needed for ESD protection solutions used at different pads. For example, a power clamp usually needs to deal with an ESD pulse in positive direction only, output pad ESD protection can be achieved using a large output buffer transistor itself, and input ESD protection may require low voltage clamping to protect CMOS gates. Nevertheless, the ESD protection
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principles remain the same, which are to create a low-impedance discharging path between every two pads to safely shunt ESD current transients and to clamp the pad voltages to a sufficiently low level. Typical ESD protection solutions for input pad are discussed in this section, of which, many may be used for other pads as well.

4.1.1 A Primary-Secondary ESD Protection Network

A classic primary-secondary ESD protection scheme is illustrated in Figure 4.1, which consists of a primary ESD protection structure, ESD_p, a secondary ESD protection unit, ESD_s, and an isolation resistor, R. A primary ESD protection unit is designed to take the majority current of ESD transients. The role of a secondary ESD protection structure is to assist the turn-on of the primary that usually has relatively higher triggering threshold as well as to ensure sufficient low voltage clamping at a pad in order to protect a CMOS gate oxide. The main function of an isolation resistor is to limit the ESD current that flows into the core circuit being protected. In operation, as an ESD appears at input pad, the secondary ESD protection unit is turned on initially at a relatively lower voltage and the ESD current flows into ground via this shunting path. As voltage builds up at the left end of isolation resistor, the primary ESD protection unit will be triggered.

![Figure 4.1 A typical primary-secondary ESD protection diagram consists of a primary protection unit, a secondary protection unit, and a current-limiting resistor.](image-url)