Chapter 5

ADVANCED ESD PROTECTION
Mixed-Signal, RF and Whole-Chip ESD Protection

Successful ESD protection design ought to take into consideration two important factors: First, ESD protection is case-dependent, e.g., process technologies, chip layout and applications, all playing roles in ESD protection design. Particularly, ESD protection for mixed-signal and RF ICs poise new challenges to IC designers. Second, ESD protection design is not about designing individual ESD protection devices, rather, it is a whole-chip design task that demands for well-planned full-chip ESD protection schemes. This chapter discusses such advanced ESD protection topics.

5.1. ESD PROTECTION FOR MIXED-SIGNAL ICs

ESD protection design for mixed-signal IC chips requires special considerations in the design procedures if one wishes to achieve an optimised protection solution at full chip level [1, 2]. Several issues should be addressed in mixed-signal IC ESD protection design. The first unique feature in mixed-signal ICs stems from the fact that multiple power supplies, i.e., $V_{DD}$ or $V_{SS}$, usually exist on a mixed-signal IC chip. It is not unusual to find a widely spread local power supply spectrum, anywhere from ±1V to ±100V. One issue associated with the multiple-supply chips is that one single type of ESD protection structure may not work for all pads across over a chip, because pad-specific customisation may be needed for optimal whole-chip protection. For example, an ESD protection structure of a trigger voltage $V_{th} = 5V$ is suitable for a $V_{DD} = 3.3V$ circuit portion, while an ESD protection device of $V_{th} = 23V$ is good for a $V_{DD} = 15V$ circuit section [3]. However, using either ESD protection structure globally may cause problem, i.e., short-circuit or slow turn-on of an ESD protection structure that may
lead to early ESD failure. A good rule of thumb in designing proper triggering voltage is to set it higher than local $V_{DD}$ with sufficient safe margins to avoid accidental turn-on of the ESD protection devices due to power bus fluctuations, while maintaining a low $V_{t1}$ for easy triggering. The key point here is to achieve optimal full-chip ESD protection, which is often not possible with a one-for-all protection structure.

The second main issue in mixed-signal ESD protection design is associated with potential accidental turn-on of an ESD protection structure in mixed-signal operation due to substantial digital noises. A rough theory follows. It is recently observed in transmission-line pulse (TLP) testing that early triggering of ESD protection devices occurs as the rise time, $t_r$, of TLP pulses decreases, which is attributed to displacement current effect due to variations in the ramping ratios of TLP pulse rising edges, referred to as the d$V$/d$t$ effect \cite{4, 5}. Further discussion over the d$V$/d$t$ effect will be given in the next section for RF ESD protection. While more research is needed to confirm the d$V$/d$t$ theory, the $V_{t1}$-$t_r$ phenomenon might cause accidental turn-on of ESD protection devices in mixed-signal operation, leading to chip malfunction. For example, it is reported that, in a mixed-signal CMOS transceiver chip, substantial digital noises were injected into the analog portion of the chip from the noisy digital circuit, resulting in noise signal with d$V$/d$t$ of $\sim 1.15 \times 10^7$ V/s \cite{6}. According to the observation and analysis to be discussed in the next section, such a high noise variation ratio may cause reduction in triggering of an ESD protection structure in non-ESD conditions. Hence, short-circuit malfunction might occur in mixed-signal ICs under normal operation. Proper design of mixed-signal ESD protection structures and special noise isolation techniques are therefore required in mixed-signal ESD protection design. Other issues may emerge in mixed-signal ESD protection design as well.

5.2. ESD PROTECTION FOR RF ICs

Driven by the amazing successes and exponential increase in demand of wireless communications, RF IC design becomes a red-hot field in semiconductor field. Consequently, a new challenge in ESD protection design emerges – ESD protection for RF ICs. However, while RF ESD becomes a popular topic in the field, one ought to ask exactly what is unique in RF ESD protection design that makes it different, if any, from ESD protection for other applications. Unfortunately, RF ESD protection is currently still a research topic in its infancy that is under heavy investigation. No well-shaped theory exists yet for RF ESD protection. Nevertheless, it is