Successful ESD protection circuit design depends upon the design approaches used. Various ESD protection circuit design methods are available, ranging from traditional trial-&-error approach, to rational, however, limited CAD-based ESD simulation method, to more accurate mixed-mode ESD simulation methodology. These ESD design approaches have different level of implementation complexity, require different degree of design experiences and knowledge, and deliver different level of design success. This chapter discusses, in depth, these various ESD protection design methodologies. Practical ESD protection design examples are provided.

8.1. ESD PROTECTION DESIGN METHODS: TRIAL-&-ERROR versus PREDICTIVE

On-chip ESD protection circuit design is a fairly complex design task because of the fact that ESD phenomena involve multiple level coupling effects, i.e., process-device-circuit-electro-thermal couplings. This multiple level coupling nature means that all these contributing factors, i.e., process, device, circuit, electro and thermal properties, must be dealt with simultaneously in an integrated fashion. Unfortunately, ESD protection circuit design is not as simple as it sounds like. Lack of proper CAD simulation tools, sufficient computing power and special ESD protection device models prevents circuit designers from performing meaningful and practical simulation during ESD protection circuit design. Currently, the experience-based trial-and-error approaches still dominate the ESD protection circuit design practices. While experience certainly plays a useful
and significantly role, solely experience-based design approach does not guarantee design successes, particularly the highly desired first-time design success. A traditional trial-and-error design approach is illustrated in Figure 8.1, where the design procedures start with defining the design specifications. With the aid of existing ESD protection design experiences, an IC designer begins design of the ESD protection circuits. Some limited and isolated ESD simulation may be performed during the design, i.e., either device level simulation or circuit level simulation. The design will be taped-out afterward and silicon wafers will be started. Testing and debugging work will be performed after receiving the silicon wafers. Should one be lucky enough, the design may work the first time. Otherwise, one has to fix the bugs and repeat the design procedures until it functions. The main problem behind the trial-and-error design approach is that, as mentioned in previous chapters, ESD protection circuit design is non-portable in nature. A proven successful ESD protection circuit design for a specific product using a specific process technology usually does not ensure functionality of an ESD protection design for a different IC chip even using the same process technology. Informal statistics indicate that it takes average three silicon iterations for an experienced IC designer to complete a successful ESD protection circuit design [1]. The main disadvantage of the trial-and-error design approach is

![Figure 8.1 A design flow chart for the traditional trial-and-error ESD protection circuit design approach.](image)

- Specifications
- Experiences
- Isolated SIM (device or circuit level)
- ESD design
- Silicon
- Test & debug
- Silicon iterations