DESIGN AND SIMULATION OF FRACTIONAL-N FREQUENCY SYNTHESIZERS

Michael H. Perrott
Massachusetts Institute of Technology
http://www-mtl.mit.edu/~perrott

Copyright © 2003 by Michael H. Perrott
All rights reserved.

Abstract

Design and simulation techniques are presented for fractional-N frequency synthesizers that allow fast and straightforward assessment of these systems at the transfer function and behavior levels, respectively. The design approach uses a freely available software tool to perform the loop filter design and allow assessment of the impact of parasitic poles/zeros, gain and pole/zero variations, and detector and VCO noise. The simulation techniques, which are also embedded in a freely available software tool, allow fast and accurate simulation of fractional-N synthesizers by leveraging an area conservation approach and by combining the VCO and divider blocks. The simulation approach is verified by comparison to measured results from a custom fractional-N frequency synthesizer IC.

1. Introduction

Fractional-N frequency synthesizers provide high speed frequency sources that can be accurately set with very high resolution, which is of significant value to many communication systems. Figure 1 illustrates this PLL architecture, which consists of a phase-frequency detector (PFD), charge pump, loop filter, voltage controlled oscillator (VCO), and a frequency divider that is dithered between integer values to achieve fractional divide ratios. The realization of fractional divide ratios allows the synthesizer to achieve very high frequency resolution. In this paper, we will focus on a particular class of fractional-N frequency synthesizers for which the divide value is dithered according to the output of a \( \Sigma-\Delta \) modulator [1,9].
Dithering of the divide value by the $\Sigma$–$\Delta$ modulator allows high frequency resolution to be achieved, but also has the negative side effect of introducing quantization noise that degrades the overall PLL noise performance [1]. It is highly desirable to be able to calculate and simulate the impact of this quantization noise, along with other noise sources in the PLL shown in Figure 2, on the overall PLL performance. It is also desirable to calculate and simulate the dynamic response of the synthesizer in response to variations of the $\Sigma$–$\Delta$ input in order to evaluate stability and characterize the performance of the system when it is used as a transmitter [2].

In this paper we will introduce design and simulation techniques for $\Sigma$–$\Delta$ fractional-N frequency synthesizers that focus on both dynamic and noise