Chapter 4

EARLY PREDICTION OF CONDUCTED-MODE EMISSION OF COMPLEX IC’S

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Abstract
A new design methodology is presented for predicting the conducted-mode emission generated by an integrated circuit. Using the Integrated Circuit Electromagnetic Model (ICEM) developed by the International Electro-technical Commission (IEC), the influence of the internal power supply distribution is modeled, and the sensitivity to design options or external factors such as supply voltage variations may be studied. Using ICEM models written in VHDL-AMS leads to efficient simulation, from the early steps of the design process, of self-perturbation and self-immunity of a complex integrated circuit. These ICEM models may be part of an IP-block definition, preserving confidentiality. Providing an early stage information on the EMC quality of the chip facilitates the way to a first-time working silicon. A full 8-bit micro-controller with core, memories and I/O blocks, from an existing industrial design, is used to validate the methodology.

Keywords: Electromagnetic compatibility, ICEM, VHDL-AMS, prediction, modeling, simulation.

1. Introduction

Early performance estimation and quality validation remains a key concern in the design of complex IC’s. IP’s definition and design reuse solve partly that problem for area, delay and even power, but characteristics like Electromagnetic compatibility (EMC) compliance is rarely addressed. Industrial designs are directly concerned with electromagnetic compatibility, particularly for portable equipments: an electronic system must be certified for given emission and susceptibility levels. Traditionally EMC compliance was only con-

sidered at the board level. This includes of course radiating effects but also simple supply transients: the $\text{di/dt}$ of supply currents will directly pollute the environment. And the higher complexity, lower dimensions and higher switching rates of modern chips will produce higher spike density on the supply rails. It becomes a real necessity to be able to estimate, from the first steps of the design process, the effect of architecture choices on EMC properties.

Till recently, the classical approach to this problem was to measure produced chips, generally in packages, to certify the design. The only correction action may be to choose another package, change some lumped elements or even re-design the chip, with a new silicon, but without any real help for the chip designer. Only recently [Steinecke et al., 2004] some comparison between models and measures, using gate level models was presented. But of course this leads to huge simulations, and requires to know the precise gate structure and routing details at the time of each simulation.

The focus of this research is to address the problem at the architecture level, as early as possible during the design process, to efficiently estimate current supply transients of a full chip, in a given package. At this level, each block is better handled as a macro-function, without precise detail of the internal structure, even if the structure is already frozen, as for example when reusing IP’s. Therefore we need an EMC model for each basic block. The model chosen is directly inspired from the ICEM model [IEC EMC Task Force, 2001]. Classically, this model is derived from measures on a packaged chip in activity, and is used to analyze the effect of the package itself on the CEM performances. Defining ICEM models at the level of the macro-function basic blocks, and assembling them in a mixed-mode simulation environment, we got a full chip CEM model. As for the classical ICEM model, the basic block CEM models are constructed to model the activity dependent current supply transients of the particular block, the digital functionality itself being modeled by classical VHDL code. The full chip simulation is then run in a VHDL-AMS environment, to allow complex stimuli to be applied, corresponding to a given digital activity. Interconnections of blocks are modeled by lumped parasitic elements, according to place and route of the blocks. To validate this model approach, the results were compared to measures in the precise case of an industrial chip, an 8-bit micro-controller. The results gives good correspondence, at reasonable computer cost.

2. **Modeling IC conducted emission**

The ICEM proposal developed in 2001 [IEC EMC Task Force, 2001] was developed to model the effect of parasitic elements of board, package and chip itself, on the spike shape of supply currents, and so helps to analyze the electromagnetic compatibility of a chip in its environment, in the domain of con-