Several chapters of this book focus on Integrated Circuit (IC) test topics. This chapter gives an overview of how loaded\(^1\) printed circuit boards are tested. While testing a modern IC can be extremely challenging, testing a board populated with 200 – 500 such devices (digital, analog and mixed signal) along with a collection of 2,000 – 3,000 analog discrete components can also pose a challenge. Boards are virtually always mixed signal or even purely analog circuits and virtually never “pure digital” designs. This greatly complicates the process and forces us to abandon well-known tools that can be used at IC test, as many such tools will not handle mixed signal designs nor designs of such magnitude. A further complication is that at board test, it is very important to locate defects, not just perform a go/no-go test.

Before jumping into the topic of board test, we need to understand what it is we are testing for. This is notably different than what we test for at the IC level, so it is an important distinction to make.

\(^1\) This does not include the topic of bare-board (unloaded board) testing. Here we assume the board itself has already been tested and that it is defect-free.

11.1 THE DEFECT SPACE AT BOARD TEST

In the early 2000s, board test engineers began to rigorously define just what a defect was [1] and something called the PCOLA/SOQ model\(^2\). In fact, the words \textit{defect} and \textit{fault} are also given rigorous definition. These may be different than the corresponding definition for an IC tester.

Rigorous definitions and a model of the important board test defects allow engineers spread across the manufacturing spectrum\(^3\) (not to mention the globe) to compare test coverage and produce metrics of test effectiveness. A designer at an Original Equipment Manufacturer (OEM) may create a circuit design specification and architecture. This may be sent to a design house where the detailed circuit design is finished. Then it could be farmed out to a layout service company that generates the actual board layout and manufacturing data. From there, it could be sent to a contract board manufacturer who will make thousands of them. But before that happens, a contract test development house may create the board test needed to assure defect-free boards are shipped. There could be a lot of independent engineers involved in this chain. If they cannot communicate about defects, this will guarantee confusion and an OEM that is at risk of missing schedules for product shipments, or the quality goals thereof.

11.1.1 What is a “Defect”?\(^4\)

A defect is an \textit{unacceptable} deviation from a norm. A defect is therefore undesirable and cause for some remedial action, from discarding the board, or repairing it, or at the very least, fixing the process step\(^4\) responsible for it. Some examples of defects are:

- An open solder joint.
- A solder joint with insufficient, excess, or malformed solder. There may be no electrical manifestation of this defect.
- A short caused by excess solder, bent pins, device misregistration.
- A dead device. For example, an ESD\(^5\) -damaged IC or a cracked resistor.
- The placement of an incorrect device.
- A missing device.
- A polarized device rotated 180 degrees.
- A misaligned device (typically laterally displaced).

\(^{2}\) The PCOLA/SOQ model is analyzed in detail in section 11.1.3.

\(^{3}\) Before the 2000s and the rush to ’outsourcing’, manufacturing and test was often all part of a vertically integrated process within a single company. Within that environment, each engineering group would work out with its neighboring groups some form of ad-hoc agreement on what was being tested and how test coverage could be measured.

\(^{4}\) Some would argue that the defect is actually in the process step. This is true from a root-cause analysis point of view. We restrict our view here to the board itself, which is what you will ship to a customer. Thus the “norm” is a contract between the manufacturer and the customer.

\(^{5}\) Electro-Static Discharge.