In recent times, the ever-evolving CMOS semiconductor design styles and the advance of manufacturing and fabrication process technologies have created a cost, schedule, yield, and throughput crisis that can no longer be efficiently handled with functional test vectors. The “Time-to-” schedule requirements coupled with modern volume requirements and nanometer defect types are eliminating the luxury of time involved in using behavioral vectors to evaluate manufacturing testing, to conduct first silicon bring-up and characterization, and to bring up yield during initial volume ramping. In addition, cost requirements are driving lower cost Automatic Test Equipment (ATE). A solution to this problem is the adoption of structural test and the use of structural testers.

This chapter introduces the concept of structural test and structural testers and delves into the adoption drivers for both and the requirements, design rules, and Design-for-Test (DFT) techniques that enable the use of the structural tester.
6.1 INTRODUCTION

Test has always been viewed as a non-value added part of the semiconductor development process. The original focus of test being to ensure that the manufacturing process produced exactly what was submitted to the fabrication facility. If the manufacturing process was error free, then test would not be required — hence, test is viewed more as an expense or a tax. To buy back some of the non-value added, test has historically been applied as a mixture of verification of the design process and verification of the manufacturing process — by the use of behavioral or functional vectors.

As semiconductor science evolved, design sizes moved from small scale integration (SSI) up through very large scale integration (VLSI) and into the System-on-a-Chip (SOC) integration levels of tens of million of transistors on a single die; wafer dimensions moved from inches to what is now a foot (300 mm); feature sizes have passed through the micron, sub-micron and into the nanometer space; and packages have grown from just a few pins to hundreds of pins. Modern designs are so rich and complex in features and in application frequencies, that it is difficult to create the functional environment needed to verify them during the design phase.

All of these advances have made the reliance on functional vectors as a method to verify the manufacturing process, a costly disadvantage. It takes longer to develop the vectors, they are more suitable for design verification, and they must be graded against fault and defect models to turn them into suitable manufacturing test vectors. Mostly though, functional vectors are costly in application on modern semiconductor ATE, also commonly known as testers. The semiconductor and the ATE are caught in an endless treadmill where the semiconductor advances, then the ATE must advance in order to test the semiconductor, then the semiconductor advances again and so on. During this advancement, as the cutting-edge semiconductors push the technological envelope, older versions branch off the relentlessly growing Moore curve to become their own markets and businesses, as shown in Figure 6-1. Devices above a certain point on the Moore curve are not driven by development costs as much as they are driven by Time-to-Market (TTM).

At some point in time the cost function of test for both the cutting-edge parts and the parts in markets all up and down the Moore curve started to exceed the cost function of semiconductor development — making the ‘cost of test’ a dominating influence on the semiconductor production process. This pushed the development of

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1 Behavioral, functional, or operational vectors are vectors that are used to exercise the development model in the software testbench to ensure that the design commits the correct actions in reference to the specification. These software simulation vectors are often converted from a software simulation format to a tester format to prove that the silicon repeats the same behaviors and operations as the software model.

2 Time-to-Market (TTM) means that there is a market window where the profit potential of the semiconductor is maximized and missing that window can result in a minimal profit or even not making enough return to break even on development and manufacturing expenses.

3 The point in time when the test cost exceeded the semiconductor manufacturing cost is different for different markets and relies on many variables, most of them manageable. The ability to conduct test cost management on the cost variables (test time, vector volume, tester...