Before delving into the discussion of the various verification techniques, we are going to review how digital ICs are developed. During its development, a digital design goes through multiple transformations, from the original set of specifications to the final product. Each of these transformations corresponds, coarsely, to a different description of the system, which is incrementally more detailed and which has its own specific semantics and set of primitives. This chapter provides a high-level overview of this design flow in the first two sections. We then review the mathematical background (Section 2.3) and cover the basic circuit structure and finite state machine definitions (Section 2.5) that are required to present the core algorithms involved in verification.

The remaining sections present the algorithms that are at the core of the current technology in design verification. Section 2.6 presents the approach of compiled-level logic simulation. This technique was first introduced in the late 80's and it is still today the industry's mainstream verification approach. Section 2.7 provides an overview of formal verification and a few of the solutions in this space; we leave the discussion of symbolic simulation and other symbolic techniques to Chapter 3.

2.1 The design flow

Figure 2.1 presents a conceptual design flow from the specifications to the final product. The flow in the figure shows a top-down approach that is very simplified – as we discuss later in this section, the reality of an industrial development is much more complex, involving many iterations through various portions of the flow in the figure, until the final design converges to a form that meets the requirements of functionality, area, timing, power and cost. The design specifications are generally presented as a document describing a set of functionalities that the final solution will have to provide and a set constraints
Figure 2.1: Conceptual design flow of a digital system