Chapter 9

SEMICONDUCTOR MANUFACTURING SCHEDULING AND DISPATCHING
State of the Art and Survey of Needs

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Abstract: This chapter discusses scheduling and dispatching in one of the most complex manufacturing environments – wafer fabrication facilities. These facilities represent the most costly and time-consuming portion of the semiconductor manufacturing process. After a brief introduction to wafer fabrication operations, the results of a survey of semiconductor manufacturers that focused on the current state of the practice and future needs are presented. Then the chapter presents a review of some recent dispatching approaches and finally an overview of a recent deterministic scheduling approach is provided.

Key words: Scheduling, dispatching, semiconductor manufacturing

1. INTRODUCTION

In recent years, both the number of applications and market demand for integrated circuits have increased dramatically. Microprocessors, memory chips, microcontrollers, and other semiconductor devices have become part of everyone’s lives: from fuel injection systems in modern automobiles, to personal computers, to cellular phones, to the projection system inside of television sets. This increased demand has in turn caused microelectronics factories (wafer fabrication facilities or “wafer fabs”) to increase their efforts to provide high-quality, on-time deliveries of affordable products to their customers. Today’s wafer fabs have been forced to become increasingly conscious of their due date performance, as dissatisfied customers now have a number of other manufacturers to turn to, should they need to find another supplier.
A number of different types of factories exist today, some of which are commodity based in that they produce a standard suite of products for general marketplace consumption. However, other factories produce application-specific integrated circuits (ASICs) for a wide array of customers. While a commodity wafer fab typically produces large quantities of a few different product types ("high-volume manufacturing"), ASIC fabs usually are tasked to produce lesser volumes of each customer's different product portfolio ("ASIC manufacturing"). Regardless of the type of wafer fab, microelectronics manufacturers strive to schedule the various orders (jobs) in their factory in such a way as to maximize on-time delivery to their customers. Companies that meet or exceed their customers' due date expectations generally have a better chance of retaining customers and receiving subsequent orders due to their previous performance. Obviously, some customer orders are more important than others.

According to the International Technology Roadmap for Semiconductors (ITRS, 2003), the cost of equipment is over 75% of factory capital costs. The ITRS indicates that, in order to utilize this equipment effectively, significant improvements in factory planning and scheduling are required. In addition to the cost pressures, today's highly competitive semiconductor markets place a greater emphasis on responsiveness to customers. In the past, competition has been primarily in the product design arena, but in the last several years high on-time delivery performance has become equally important for competitive success. Good delivery performance consists of order lead times that are both short and reliable. This can be achieved through either good production scheduling or using inventory to buffer customers against lengthy manufacturing delays. For a variety of reasons including holding costs and potential obsolescence, the latter option is becoming less attractive to semiconductor manufacturers. Thus, a recent thrust of manufacturing management has been on using effective scheduling techniques as a vehicle to achieve a competitive advantage.

Scheduling semiconductor manufacturing facilities is a very difficult problem and is among the most complex scheduling problems encountered today. Uzsoy, Lee, and Martin-Vega (1992) provide an excellent description of the semiconductor manufacturing process, placing scheduling in the context of production planning and fab performance evaluation. Wafer fab scheduling is a challenge that has yet to be tackled in a completely satisfactory manner. There are six main features that complicate scheduling these systems: large number of processing steps, re-entrant flows, batch tools, random equipment failures, sequence-dependent tool setups, and the fact that some processing steps require auxiliary resources (e.g. reticles).

In a typical wafer fab, there often are dozens of process flows. Each process flow contains 300-500 processing steps and more than one hundred