Chapter 7

Digitization of the inter-die interface

In the previous chapter, alternative solutions for the digitization of the conditioning channel have been presented. In practice, the conditioning channel may extend over multiple dies, possibly in a different technology. The ADC can be integrated with the analog part or it is put on the digital die. Depending on this partitioning choice, the inter-die interface will be digital or analog. It is shown in this chapter that the digitization of the conditioning channel leads to a digitization of the inter-die interface as well. This is depicted in fig. 7.1.

The chapter starts with some general considerations on the choice of the interface. Next, possible IC partitioning scenarios for a $\Sigma\Delta$ based conditioning channel are compared with respect to power consumption in the associated interface. The analysis on power consumption supports the on-going digitization of the inter-die interface for high-resolution conditioning channels.

7.1 Considerations

In case of a multi-die solution, the choice for an analog or a digital interface can be determined by a number of factors, a.o.:

- technology choice for ADC/cost: The ADC can either be integrated in an advanced CMOS technology or a technology with high-performance analog capabilities. Often, the choice for one or the other is cost-driven.

- electro-magnetic interference: In case of a digital interface the communication can be a source of electro-magnetic interference affecting the performance of other circuits. The opposite is true for an analog interface: it is susceptible to interference from other sources. A differential implementation is therefore preferable in all cases. For a digital interface low-swing operation is favored while for an analog link a large signal is preferred.
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Figure 7.1: Analog interface for a full-analog conditioning channel (a) and digital interface for a full-digital channel

- **pin count:** An analog, differential interface requires two pins per signal path. The same is true for a digital, differential interface. Likely, though, it needs many more signal paths because of the number of parallel output bits. These bits can be serialized to reduce the pin count. Next to the serializing/de-serializing this also requires one additional signal path to transmit a synchronization signal. In addition, a digital interface requires transmission of the clock, unless clock recovery is implemented.

- **standardization:** In an industrial realization, compatibility of the analog die with various digital ICs and vice versa is of major importance. As a consequence, the inter-die interface is being standardized for various applications. This argument is illustrated for the example of a GSM chip set.

  **Partitioning of a GSM chip set:** Fig. 7.2.a shows a typical chip partitioning for the GSM chip-sets of the 1990’s: it has an analog interface between the RF IC and the digital baseband with the ADCs and DACs. Meanwhile, a consortium of companies is defining a digital interface standard “DigRF” for the next generation of GSM solutions (see fig. 7.2.b and [86]). Similarly, standards like a.o. ‘MiPi” [87], “JC61” [88] and “BlueRF” are being developed.

- **power/performance of the interface:** A last argument for choosing a digital or an analog interface is in their different power/performance relation.

This is analyzed next. The analysis of the interface is conducted from the angle of digitization of the channel. Hence, it is of a limited nature.

### 7.2 Power in the interface

In a $\Sigma A$ based conditioning channel the IC partitioning can be such that the inter-die interface is either analog (before the ADC), digital after decimation or digital but before decimation (see fig. 7.3). The power associated with these three possible interfaces is