Chapter 2

WIRES AS INTERCONNECTS

Li-Rong Zheng and Hannu Tenhunen
Royal Institute of Technology (KTH), Stockholm, Sweden
lirong@imit.kth.se, hannu@imit.kth.se

Abstract: Deep submicron technology is rapidly leading to exceedingly complex, billion-transistor chips. This has resulted in a new circuit paradigm - system-on-chip (SoC). However, deep submicron physics indicates that wires, not transistors, dominate power and performance. Interconnects have been a key design objective in deep submicron SoC. In this chapter, we review interconnect performance as technologies migrate from 0.25\(\mu\)m to 0.035\(\mu\)m feature sizes. Challenges of deep submicron effects and their impacts on advanced chip design are summarized. Basic concepts of signal integrity and various noise sources in deep submicron SoC are illustrated. Finally, interconnect strategies and interconnect-centric design methodologies are generally described; various design techniques for signal and power integrity in deep submicron SoC are discussed.

Key words: Interconnects, deep submicron CMOS, signal integrity, power integrity

1. EVOLUTION OF MICROELECTRONICS TECHNOLOGY

1.1 Moore’s Law and Technology Scaling

In 1958, Jack S. Kilby, an employee of Texas Instruments, created the first integrated circuits [1], which were, of course, very crude as measured by today’s standards. Since then, with the rapid development of processing technology, particularly in lithography, the number of components of a chip increased very rapidly. With this pioneer work, Kilby earned the Nobel Prize in 2000.
In the beginning of the 1960’s, shortly after the invention of the IC, Gordon Moore, one of the pioneers in Silicon Valley, formulated an empirical law stating that the performance of an IC, including the number of components on it, doubles every 18-24 months with the same chip price. This became known as Moore’s law. Remarkably enough, it is still holding up after forty years, and this trend is likely continuing for the next 10 years, as shown in Figure 2.1. Today, the mainstream technology for IC fabrication has already been in deep submicron (DSM) regime, and the increased integration capacity has resulted in exceedingly complex chips such as system-on-chip (SoC).

Figure 2.1  Evolution of microelectronic technology that has so far followed Moore’s law very well. For the future, there are different extrapolations, depending upon assumptions on the development of the process technology. Also shown in the figure are the rapid development of process technologies and the size of the silicon wafers.

1.2 Deep Submicron Effects

The system-on-chip design paradigm and deep submicron technology bring two main challenges to the ASIC design community. The first challenge is productivity, i.e., the ability to use millions of gates within the ever shorter time-to-market, which is currently tackled with the design methodology based on Intellectual Property (IP) right blocks. The second challenge is coping with

* The data of this figure are from several sources. Historical data are based on surveys, including that from SCS (www.semiconsulting.com). Future trends are based largely on projections by the NTRS’97 and ITRS’99. The division of LSI, VLSI, ULSI, and GSI is based on some publications.