4 Oxide Reliability Issues

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In this section, we will describe and discuss the electric reliability of thin oxide layers (range 1.5–15nm). An overview is presented of the ideas that have been proposed in the past decade to evaluate, model and predict the oxide reliability.

First, we will describe the oxide wear-out phase, that is the gradual degradation of the electrical properties of the oxide under electrical stress. Second, the oxide breakdown phenomenon is discussed with special emphasis on soft breakdown issues in ultra thin layers. Third, the reliability prediction methodology is addressed.

4.1 Thin Oxide Layer Degradation Under Electrical Stress

The reliability of oxide layers is typically tested by applying either a constant voltage stress (CVS) or a Constant current stress (CCS) to a capacitor. The thin SiO$_2$-dielectric gradually degrades until breakdown occurs. We can think of thin oxide layer degradation by electrical stress as the continuous generation of trapping centers in the bulk of the oxide. Breakdown is triggered when the accumulated damage reaches a critical level.

During oxide stress, several phenomena can be observed: interface trap creation (Sect. 4.1.1), negative and/or positive charge trapping (Sect. 4.1.2), hole fluence (Sect. 4.1.3), neutral electron trap creation (Sect. 4.1.4), and the generation of a Stress-Induced Leakage Current (=SILC) (Sect. 4.1.5). These properties are important monitors during oxide stress, and can help one understand the degradation mechanisms. The trap generation mechanism itself is discussed in Sect. 4.1.6.

Several research groups have proposed breakdown models that directly correlate one of these properties with breakdown. The line of thought is common to all models: some damage-related parameter exceeds a critical threshold at the moment breakdown is triggered.

An important observation is that a relation between accumulated oxide damage and breakdown is only found for the intrinsic breakdown mode. Extrinsic breakdown is determined by localized, process-related physical phe-
nomena that do not influence in measurable way the global degradation phenomena.

4.1.1 Interface Trap Creation

During high field oxide stressing, interface traps are created at the substrate/oxide interface [4.38, 4.40]. Their density can be obtained either from CV-measurements [4.74], or, on transistors, from charge-pumping measurements [4.50]. Recently, interface trap-related low voltage Stress-Induced Leakage Current in sub 3.5 nm oxides has been used to quantify the interface trap density [4.49].

It has been claimed that the interface trap density, $D_{it}$, reaches a critical density, $D_{it, crit}$, at the moment of oxide breakdown. In earlier work, the triggering of breakdown is suggested to be caused by a local interface softening due to accumulation of traps [4.38], but more recently, the critical interface trap density is merely viewed as a monitor for the total density of traps in the oxide. By means of a percolation model [4.29, 4.32, 4.111] (see also Sect. 4.2), the interface trap density can be related to this total bulk trap density [4.43].

4.1.2 Oxide Charge Trapping

In oxides with thickness larger than 4 nm, a typical observation during a high field CCS is the initial decrease of the applied voltage needed to force the required current, followed by a voltage increase which can become larger than the initially applied voltage [4.37, 4.38].

The voltage shifts are caused by charge trapping (initially positive, then negative charge) in the oxide, leading to an oxide field distortion and subsequent change of the tunnel current density. During a CVS, exactly the opposite current shifts are measured, i.e. an initial increase of the current followed by a decrease.

In sub-4 nm oxides, the charge built-up almost completely disappears. Typically, as illustrated in Fig. 4.1, a very small increase of the stress current during CVS is measured, which is attributed to positive trapping and the gradual generation of a SILC [4.77].

In some older publications [4.14, 4.16], it is claimed that the positive charge trapping in the oxide is responsible for triggering the breakdown event. During e.g. a CCS a locally enhanced charge trapping will not influence the total current density in the capacitor, but will lead to a local current density increase, resulting in an increased stress, which in turn leads to an increased positive charge trapping. In this way a positive feed-back mechanism is initiated that finally results in breakdown.

Two arguments oppose this idea: (i) In ultra-thin sub-4 nm oxides the measurable positive charge trapping is extremely small and yet, the oxides break down. (ii) The possible role of the negative charge in the oxide is