New Simulations between CRCW PRAMs

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Abstract: This paper is part of a continued investigation of the relative power of different variants of the CRCW PRAM with infinite global memory. The models that we consider are the standard PRIORITY and COMMON PRAMs, together with the less well-known COLLISION+ and TOLERANT PRAMs. We describe several new results for the simulation of an n-processor PRIORITY PRAM on weaker machines:

1. Introduction

The PRAM is one of the most popular models of parallel computers. A PRAM consists of a collection of sequential processors numbered 1,...,p and operating synchronously on a global memory, which in this paper will be assumed infinite. Various PRAMs have been introduced, differing in the conventions regarding concurrent reading and writing, i.e., attempts by several processors to access the same memory cell in the same step. CRCW (concurrent-read concurrent-write) PRAMs allow simultaneous reading from as well as simultaneous writing to each cell. Simultaneous writing is not immediately logically meaningful, and various different rules for the

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resolution of write conflicts have been introduced and used in concrete algorithms. The conflict resolution rules of interest to us are:

**COMMON [K]:** All processors writing to a given cell in a given step must be writing the same value, which then gets stored in the cell;

**TOLERANT [GR]:** If more than one processor attempts to write to a given cell in a given step, then the contents of that cell do not change;

**COLLISION+ [CDHR]:** If the processors attempting to write to a given cell in a given step all attempt to write the same value, then that value gets stored in the cell; if at least two values differ, a special collision symbol is stored in the cell;

**ARBITRARY [SV]:** If several processors simultaneously attempt to write to a given cell, then one of them succeeds and writes its value, but there is no rule assumed to govern the selection of the successful processor;

**PRIORITY [G]:** If several processors simultaneously attempt to write to a given cell, then the lowest-numbered processor among them succeeds.

This paper continues the investigation, begun in [CDHR], of the relative power of different CRCW PRAMs.

For brevity, a CRCW PRAM working according to the COMMON (TOLERANT, etc.) rule will be called a COMMON (TOLERANT, etc.). The number of processors of a particular machine is indicated by a postfixed integer in parentheses (e.g., PRIORITY(n) denotes a PRIORITY PRAM with n processors). A simulation by one PRAM M2 of a single step of another PRAM M1 is a computation by M2 that changes the state of M2's global memory exactly as the single step under consideration changes the state of M1's global memory (i.e., it implements the same state transition). As a technical requirement, we assume the simulating machine M2 to have an additional infinite global memory that can be used to hold the variables of the simulation (if an upper bound on the space used by M1 is easily computable, an upper segment of a single memory can be used for the same purpose). We say that M2 simulates M1 with slowdown T if at most T steps of M2 are needed to simulate a single step of M1.

As observed in [CDHR], some relations between the CRCW PRAM models defined above are obvious. For instance, ARBITRARY is stronger than COLLISION+ in the sense that COLLISION+(n) can be simulated on ARBITRARY(n) with slowdown O(1). If we express this fact as "COLLISION+ ≤ ARBITRARY", then the following partial ordering is easy to establish:

\[
\begin{align*}
\text{COMMON} & \preceq \text{COLLISION+} \preceq \text{ARBITRARY} \preceq \text{PRIORITY.}
\end{align*}
\]

Grosmusz and Ragde [GR] proved that COMMON is not comparable with TOLERANT in the sense of this relation “≤”.

In this paper we contribute several new efficient algorithms simulating PRIORITY (the strongest commonly used CRCW PRAM) on the weaker models COMMON, TOLERANT and COLLISION+. New and previously known simulation results are summarized in Table 1.