Some Remarks on the Test Complexity of Iterative Logic Arrays

(Extended Abstract)

Bernd Becker* Joachim Hartmann**

Abstract

The problem of detecting single cellular faults in arbitrarily large (one-dimensional, unilateral, combinational) iterative logic arrays (= ILAs) is considered. We prove that the test complexity of such an ILA is either constant or linear in the length of the ILA. The determination of the test complexity and the specification of the test set can be carried out by algorithms whose complexity only depends on the individual cell function of the ILA. Fault patterns which characterize any cellular fault are defined and their testability properties like (full, partial) testability, redundancy, test complexity are studied to give insight into the testability properties of the ILA under test construction.

1 Introduction

Iterative arrays are becoming increasingly popular with the advent of very large scale integration (VLSI) and wafer scale integration (WSI). The manufacturing of large array systems for use e.g. in arithmetic logic units, parallel multipliers and dividers, signal processing, pattern recognition, bit-sliced systems ([16,15,13]) is now manageable. Advantages such as simplified design, layout and testing have motivated research on the capabilities of ILAs since the beginning of the sixties [11,12,18,5,17,20]. We focus on testability aspects of iterative structures in this paper. Before going into the details we want to emphasize the practical relevance of testing problems by making some general remarks. For a comprehensive treatment of the topic see e.g. [21].

As a result of technological improvements, VLSI electronic circuitry may nowadays contain hundreds of thousands of transistors on a single silicon chip. Even if the chips are correctly designed, a non negligible fraction of them will have physical defects caused by imperfections occurring during the manufacturing process (e.g., open connections induced by dust particles). Therefore, there has to be a test phase in which the “good” chips are sorted from the “bad” ones.

*Computer Science Department, J.W.G.-University, 6000 Frankfurt, Germany. The research reported has been supported in part by DFG, Grant 1176/3-1.

**Computer Science Department, University of Saarland, 6600 Saarbrücken, Germany
Because of the variety of physical defects restrictions on a subset of the possible faults are necessary; these simplifying assumptions based on the experience of many years are manifested in fault models. For this paper, we adopt the cellular fault model (CFM). This is the strongest cell-based fault model to control the correct static behaviour of a combinational circuit; it tries to completely verify the function of each basic cell in the circuit [9,4]. Furthermore, it is as usually assumed that there is at most one fault (according to the CFM) in the circuit (= single fault assumption).

In spite of these restrictions the test generation problem for general Boolean circuits is easily seen to remain NP-complete from the theoretical point of view. This relates to the following observations in practice. With increasing complexity of VLSI circuits, the costs for the test phase have risen dramatically, at least 25% and up to 60-70% of the total product costs count on testing [14,19]. Therefore, subclasses of circuits which, due to their structural properties, allow efficient test generation algorithms and as a result yield complete test sets of small size have to be classified and investigated. Typical examples are memories, arithmetical units and linear or tree-like structures (see e.g. [1,7,10,8,4,2,3]).

In the context of this paper we restrict our attention to iterative array structures. The first paper in this context authored by Kautz appeared in 1967 [12] and intialized research activities which led to numerous extensions and variations of the results presented there. For a good overview see e.g. [20,6,13,17]. Common to almost all these papers is the following approach: under varying assumptions sufficient conditions to ensure C-testability, i.e. complete testability with a number of tests that only depends on the basic cell types of the array and is independent of the common size of the array, are derived. If an array does not fulfill these properties, modifications of the basic cells are proposed to guarantee C-testability. Of course, these modifications must not destroy the original behaviour of the cells and should cause minimal overhead. The sufficient conditions given are directed to allow modifications with small overhead, but normally they are not necessary. In general, it turns out to be very difficult to characterize C-testable ILAs by necessary and sufficient conditions. For some classes of two-dimensional arrays elementary problems in the test generation process such as the controllability problem even turn out to be undecidable, if they are to be solved uniformly for all arrays in the class [11]. Problems of this type do not occur if one only considers one-dimensional arrays.

More precisely, it is the purpose of this paper to point out that the testability properties of one-dimensional, horizontally connected, unilateral, homogeneous, combinational ILAs can be completely characterized. (From now on the term ILA is to be interpreted in this sense. Especially notice that only one basic cell type is used to build up the ILAs.) Our investigations are a continuation of the fundamental work done by Kautz [12] and later by Friedman [9]. We shortly review the main results of both papers and then come to the generalizations obtained in this paper. Kautz and Friedman as well make the assumption that the ILAs under test are fully testable, i.e. redundant faults do not occur. Kautz then characterized the ILAs which are testable with \( NM \) input patterns. \( NM \) is the total number of input patterns to the basic cell considered and, since in a fully testable ILA all possible