ATTEMPT-1:  
A Reconfigurable Multiprocessor Testbed

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Abstract. The future advanced technologies of devices will enable to implement some number of processors into a single chip. We call such a chip the multiprocessor-chip. In such a multiprocessor-chip, architectural trade-off is completely different from current bus connected multiprocessors. In order to emulate such future multiprocessors, a reconfigurable testbed multiprocessor ATTEMPT-1 is proposed. By using programmable devices (CPLDs and FPGAs) in the core of the system, various parameters of the cache and bus system are selectable. Since the each core of controller is described in the HDL (Hardware Description Language) and implemented on CPLD, cache protocols and bus protocols can be changed just by rewriting description on the state transitions. By using high speed FPGAs in the data path, enough high speed (25MHz clock) is kept in spite of its flexibilty.

1 Introduction

A bus connected multiprocessor is one of the most promising types of small scale parallel machines because of its simple and economical structure. Usually, all processors share a common address space of the shared memory. In order to reduce the access latency and the bus congestion, each processor provides a private cache with a snoop mechanism[1].

The existing snoop cache structures and protocols are optimized for the current level of technologies: the access frequency of the processor, the transfer speed of the backplane bus, access latency of the SRAM used in the cache, and the bandwidth of the DRAM used in the shared memory.

However, the future advanced technologies of devices and implementation will change the structure of such bus connected multiprocessors. Some number of processors and caches will be implemented on a single chip. We call such a chip the multiprocessor-chip. Fig.1 shows the structure of the target multiprocessor-chip.

In this implementation, the speed of bus inside the chip is far faster than that of the backplane bus, and the large gap of the bandwidth between inside and outside the chip will become a substantial problem.
We have studied on a memory and communication architecture optimized for such a multiprocessor-chip[2]. The proposed cache system is designed so as to make the best use of high bandwidth of internal bus, and the communication with outside shared memory is minimized. The synchronization and message passing mechanisms are also combined into the cache to minimize the shared memory access.

The performance of the proposed cache system has been evaluated using a software instruction level simulator[3], and architectural trade-off is researched. However, it takes a long time to evaluate with practical parallel applications using such a software simulator. Furthermore, The influence of the operating system which sometimes affects the performance cannot be evaluated on such an environment.

Using a real machine which provides a measurement facility, the performance evaluation with practical parallel applications on an operating system can be quickly performed. Our first multiprocessor testbed ATTEMPT-0[4] was designed and used for this purpose. However, in the usual testbed, the size, operating speed, and protocol of the cache and bus system are fixed in the current art of technology. Since the future technologies for multiprocessor-chips are not fixed, it is required that the parameters of the cache system can be changed in the wide range.

In order to cope with this problem, a reconfigurable multiprocessor testbed ATTEMPT-1 is proposed. By using programmable devices (CPLDs and FPGAs) in the core of the system, various parameters of the cache and the bus system are selectable. Since the core of the controllers are described in the HDL (Hardware Description Language) and implemented on CPLDs, cache protocols and bus protocols can be changed just by rewriting description on the state transition-s. Although high degree of flexibility sometimes degrades system performance, ATTEMPT-1 operates an enough speed for evaluations (25MHz clock).

For achieving a practical performance with maximum flexibility, high speed discrete devices are used in a large part of ATTEMPT-1, and the FPGA/CPLDs are used only in the core of the system.

2 Overview of ATTEMPT-1

As shown in Fig.2, processor boards, each providing a RISC processor and a snoop cache are connected with shared memory boards by a shared bus in ATTEMPT-1. Although the structure of ATTEMPT-1 is mostly like current