CAD-oriented FPGA and Dedicated CAD System for Telecommunications

Toshiaki Miyazaki, Atsushi Takahara, Masaru Katayama, Takahiro Murooka, Takaki Ichimori†, Kennosuke Fukami‡, Akihiro Tsutsui§, Kazuhiro Hayashi§§

NTT System Electronics Laboratories
A1-329S, 3-1 Morinosato Wakamiya, Atsugi, 243-01 JAPAN
e-mail: miyazaki@aecl.ntt.co.jp
† NTT Network Service Systems Laboratories
‡‡ NTT Science and Core Technology Laboratory Group
§§ NTT Optical Network Systems Laboratories

Abstract. This paper describes a newly developed FPGA and its dedicated CAD system. The FPGA is an improved version of our previous telecommunication-based FPGA, especially in terms of the routing resource architecture. Thus, in addition to having the good features of our previous FPGA for realizing telecommunications circuits, it enables us to adopt a top-down design methodology for application circuits configured in the FPGA. The architecture is determined based on a quantitative evaluation carried out to balance the FPGA with CAD algorithms.

1 Introduction

Today, more functions are needed in each protocol layer to realize flexible multimedia services in digital telecommunication networks [1]. However, current telecommunication systems are often constructed by dedicated hardware. This is because data transmission requires high throughput and various bit-level manipulations must be performed, which CPUs or DSPs cannot handle well. So, the implementation of telecommunication circuits is far from rich in terms of flexibility. To remedy this situation, we have developed a telecommunication-based FPGA called PROTEUS [2] and reconfigurable telecommunication systems utilizing it [3]. PROTEUS was developed based on analytical results for telecommunication circuits [4], which have the following characteristics;

- relatively many latches compared to the amount of combinational logic,
- a lot of pattern matching operations, and
- strong directions in the main data streams.

Thus, application circuits related to telecommunications can easily perform real-time operations with the PROTEUS FPGA. Unfortunately, the logic vs. routing resource balance in PROTEUS was not optimal, and its dedicated CAD system [5], especially the router, suffered from a lack of routing resources. To
overcome these problems, we have newly designed a well-balanced FPGA using a FPGA/CAD co-evaluation system called FACT [6]. The FPGA architecture has been improved to the point where the CAD system can easily handle it without sacrificing the good features of the original PROTEUS when the user designs an application circuit.

In this paper, how we decided upon the new FPGA architecture is described first. Next, we introduce newly developed FPGA, which is called PROTEUS-Lite. Finally, its dedicated CAD environment with some experimental results is discussed.

2 Quantitative Analysis

The PROTEUS-Lite architecture was determined quantitatively, using FACT system [6]. FACT is an FPGA/CAD co-evaluation system. It can simulate ordinary circuit-design processes for FPGAs such as technology mapping, placement, and routing. In addition, the user can define a new FPGA architecture using the Architecture Definition Format (ADF) provided in FACT system.

A routing bottleneck often occurs at the inputs or outputs of each logic block, which is called Basic Cell, or BC, in PROTEUS and PROTEUS-Lite. Thus, we concentrated on improving the routing topology around the BCs.

First, we considered the three architecture types shown in Fig. 1. Each type has a symmetrical array structure. However, the input and output directions to/from each BC differ among the three types. In type A, the inputs come from both the left vertical and upper horizontal routing channels, and the outputs go to both the right vertical and upper horizontal channels. In type B, the inputs come only from the upper horizontal channel, and the outputs also go to it. In type C, both the inputs and outputs are connected to the upper and lower horizontal channels. Six circuits were applied to the above architectures while the numbers of tracks in the vertical and horizontal channels and switch pattern in each switch box were changed.

We evaluated a total of 23 architectures in the three categories. The results are shown in Fig. 1. In the graph, the y-coordinate indicates the number of unrouted nets and the x-coordinate indicates the number of switches in each cyclic pattern in the FPGA, i.e., the switches in several switch boxes. The two numbers in parentheses are the numbers of horizontal and vertical tracks in each routing channel. The target area had less than 450 switches per one cyclic pattern and less than ten unrouted nets. These were not strict constrains; they were decided from the standpoints of hardware cost and CAD aspect.

In one type A architecture, all nets are completely routed, i.e., the number of unrouted nets is zero. The architecture has complete connection switches that can connect any two tracks coming into the same switch box. Thus, we concentrate only on the width of each channel, and the routing results indicate that the architecture has enough channel width (in this case, twenty) to route the circuit data. However, this architecture requires too many switches. So, we also