Chapter 11

HIGH-SPEED IO DESIGN

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Abstract: This chapter explores common methods and circuit architectures used to transmit and receive data through off-chip links.

Key words: High-speed IO; off-chip links; serial data transfer; parallel data bus; FR-4; skin effect; dielectric loss; clock phase alignment; derived clocking; source synchronous; forwarded clocking; plesiochronous; mesochronous.

1. Introduction

In order for system performance to keep pace with the ever-increasing speed of the microprocessor, the bandwidth of the signaling into and out of the microprocessor must follow the trend in on-chip processing performance. However, the physical limitations imposed by the interconnect channel, which exhibits increasing amounts of signal loss and jitter amplification at higher frequencies, impedes the increase in off-chip signaling speed. Numerous strategies to cope with the interconnect properties have been developed, enabled by more sophisticated techniques to control and process the off-chip electrical signals.

This chapter discusses the most prevalent of these techniques, focusing on the chip-to-chip communication topologies common for microprocessors, namely access to memory, processor-to-processor communication for parallel computing, and processor-to-chipset communication. These links generally run over short distances of up to one or two meters and consist of buses of parallel data lanes carrying wide data words. Although serial communication shares many of the same properties and techniques as the parallel bus designs, serial...
communication, which generally takes place over much longer distances, will not be discussed explicitly here.

Our discussion begins with a comparison of the on-chip and off-chip data transmission environment, with an emphasis on the desired properties of the off-chip communication system. Several common signaling methods will be shown. We then explore the properties of the off-chip signaling medium, particularly those that dominate at high frequencies and therefore limit off-chip signaling speed. Techniques and example circuit topologies for adapting to these effects in both the time and voltage domains, as well as their limitations, are shown.

2. IO Signaling

The overall function of IO is to faithfully convey data from a transmitter chip to a receiver chip [5, 8]. Similar to on-chip communication, where data is passed from one section of the chip to another, off-chip communication must define the data representation for a “1” and a “0.” It must also transmit the output data and capture the input data synchronously so that the input data stream can enter the synchronously clocked logic on the receiver side.

A typical configuration for microprocessor IO is shown in Figure 1. It depicts the processor in communication with a variety of external components, such as memory, a memory chipset, another processor, and a chipset communicating with external storage and networking devices. Off-chip communication takes place through a variety of parallel data buses. Each data bus consists of several parallel data lanes conveying information through an interconnection wire.

![Figure 1. Typical components connected to a microprocessor.](image)