Chapter 9

MICROPROCESSOR ARCHITECTURE FOR YIELD ENHANCEMENT AND RELIABLE OPERATION

Hisashige Ando
Fujitsu Ltd., 4-1-1 Kamikodanaka, Nakahara-ku, Kawasaki, Japan 211-8588

Abstract: With the advance of semiconductor scaling, smaller devices become more vulnerable to an SEU (single event upset, i.e. neutron hit etc.) and operating margin of the circuits is reduced both due to reduced operating voltage and larger process variations. Robust circuit design alone cannot solve these problems. Micro-architectural techniques for avoiding defects and error detection and correction microarchitecture can significantly reduce the probability of failure and enhance the yield and the reliable operation of a microprocessor. The failure mechanisms of nanometer class semiconductor VLSI circuits are described as a background. Then concept and methods of error detection and correction are described, followed by microarchitecture/logic design error detection and recovery techniques. Commercial microprocessors using error detection and recovery techniques are also presented.

Key words: redundancy; error detection; error correction; checkpoint; microprocessor.

1. Introduction

Microprocessors have been taking advantage of continuing semiconductor scaling, from Intel 4004 microprocessors introduced in 1971 containing only 2300 transistors to recent processors integrating more than 1 billion transistors. Semiconductor scaling reduced the minimum feature size of mass-production integrated circuits down to 90 nm in 2004 and the scaling trend is expected to continue down to 22 nm in 2016.
However, CMOS semiconductor scaling becomes harder and harder as it
ears the end of scaling due to fundamental physical limits. As the feature size
becomes smaller, a smaller dust particle can cause fatal defects, which lowers
the yield of a chip. Also smaller features are harder to control and the electrical
parameter variation in the chips becomes larger. This also lowers the yield of
the chips.

Smaller transistors and reduced supply voltage reduce the operating margin
of the circuits as the noise margin is mostly proportional to the supply volt-
age and the parameter variation of the smaller devices is larger. Electrostatic
charge stored in a circuit node decreases rapidly as device sizes and voltage
are reduced. This makes circuits more susceptible to an alpha particle and a
neutron hit as the charge generated by a hit is constant and does not scale with
the shrinking geometry.

Circuits must be designed to accommodate larger device parameter vari-
tions, but it is inefficient to design circuits robust enough to accommodate very
large parameter variations or to withstand neutron hits.

Microarchitectural approaches, for repairing fixed errors and recovering
from transient errors, are becoming important means to enable microprocessors
and/or other VLSI systems to be manufactured economically and to operate
reliably.

2. Semiconductor Scaling Issues

2.1. Device Parameter Variation

In a photolithographic process, the intensity of the light, focus, sensitivity
and thickness of photo-resist etc. affect the size of the patterns exposed. In other
processes, variations in the mixture and flow rate of gases, process temperature
and so on, affect the thickness of a film or diffusion of impurities. Although
equipment manufacturers and semiconductor engineers are working hard to
reduce these variations, it is a tough battle to keep device parameter variation
small in line with the continuing scaling.

As the feature size becomes smaller than the wavelength of light, the inter-
ference of light affects the intensity of exposure and distorts the pattern to
be exposed. OPC (optical proximity correction) is used to compensate this
distortion, but the residual distortion becomes the source of device parameter
variation [1–3].

The light used for the photolithographic process is a beam of photons.
Near the edge of a line some roughness cannot be avoided as the photons
hit the photoresist like bullets. As the line width (which defines gate length)
becomes narrower, rough edges occupy an increasing percentage of the line
width [4]. As the length of the transistor channel becomes a few tens of