# Chip Level Testing

CHAPTER 15

*And will you succeed? Yes indeed, yes indeed! Ninety-eight and three-quarters percent guaranteed!*

*Dr. Seuss*

Testing at the block level is common. Testing at the system level is necessary. As you probably know, it's the system level interaction between the various blocks that must be tested. This system level interaction is the focus of this chapter.

This chapter presents three main concepts:

- The chip now has four UART interfaces.
- We develop three tests, showing a progression from getting the interfaces running to a generic test with irritators.
- We can adapt the original block-level test to be used in the system.

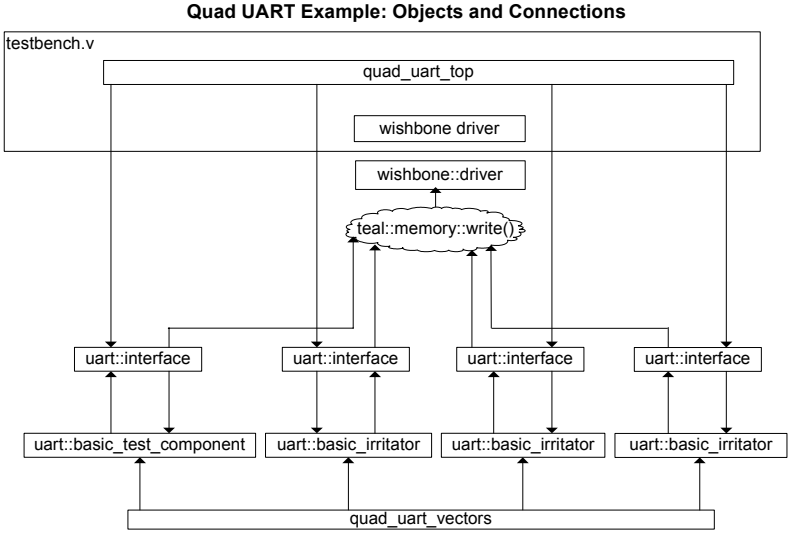
## Overview

This chapter highlights Truss irritators. We'll adapt the UART block-level testbench to a system-level testbench that has four UARTS. One of these UARTS will be randomly chosen to be the focus of the test, while the other three will serve as background traffic irritators. While this chapter uses UARTs for the irritators, the idea is generic.

## Theory of Operation

This verification system builds upon the block-level UART system. We will adapt the components developed in the last chapter, and add a few new tests. These tests will show how irritators are used.

Here are the main components involved in the simulation:




One difference from the block-level system is that the testbench now does not directly build each of the four UART interface's objects (such as the generator, checkers, agents, and so on). This is left to the