10.1 INTRODUCTION

The demand for portable electronic devices is growing rapidly and, due in large part to the development of wireless communications, is expected to continue to grow. This demand has generated great interest in low power design, which initially focused on controlling dynamic power consumption. While this focus resulted in significant improvements in dynamic power efficiency, two issues subsequently arose which rendered this initial focus inadequate. The combination of these two issues has motivated the development of leakage reduction techniques and related design automation.

The first issue pertains to the operational characteristics of wireless devices – basically, their operation tends to be bursty. That is, relatively short periods of activity are followed by relatively lengthy periods of inactivity, and while the power consumption during the active period is dominated by dynamic power, the power consumption during the inactive period (known as standby or sleep mode) is dominated by leakage power.

The second issue pertains to leakage power itself. Leakage is increasing exponentially with each new process generation due to the scaling of transistor threshold voltages [19].

This chapter will describe in detail the use of power gating for leakage reduction along with cell-based design automation methods employed by the CoolPower™ design tool, and is organized as follows. The next section briefly surveys different leakage reduction techniques, providing the motivation for power gating. The subsequent sections describe design issues, CoolPower automation methods including analysis and optimization techniques, and two different power gating application flows as well as results from using those flows. This chapter then concludes with a view to the future and likely new developments in power gating design.
10.2 LEAKAGE CONTROL TECHNIQUES

This section briefly presents and compares several different leakage control techniques to enable the reader to understand the motivations for the development and deployment of MTCMOS power gating.¹

Leakage has several different components, however the largest components are sub-threshold related [11]. The equation for sub-threshold leakage current is

$$I_{leakage} = I_{s0} e^{(V_{gs} - V_{th0})/nV_T} (1 - e^{-V_{ds}/V_T})$$

(10.1)

where

$$I_{s0} = K(W_{eff}/L_{eff})V_f^2$$

(10.2)

$$V_{th} = V_{th0} - \gamma V_{bs} - \eta V_{ds}$$

(10.3)

and $V_{gs}$ is the transistor-gate to source voltage; $V_{ds}$ is the drain to source voltage; $V_{th0}$ is the zero bias threshold voltage; $\gamma$ is the linearized body effect coefficient; $V_{bs}$ is the source to body voltage; $\eta$ is the DIBL (drain induced barrier lowering) coefficient; $n$ is the subthreshold swing coefficient; $V_T$ is the thermal voltage; $K$ is a process constant; $W_{eff}$ is the effective transistor width; and $L_{eff}$ is the effective transistor channel length. [7][15]

Leakage control techniques focus on controlling one or more terms in these equations. The most prevalent techniques can be categorized as reducing $V_{gs}$, increasing $V_{th0}$, lowering $V_{bs}$, and reducing $V_{ds}$. Several different methods for controlling these terms are described below along with how they relate to equations (10.1) to (10.3).

10.2.1 Reverse Body Bias (RBB)

Since leakage currents are a function of the device thresholds, one method for controlling leakage is to control $V_{th}$ through the use of substrate, or body, bias. In this case, the substrate or the appropriate well is biased so as to raise the transistor thresholds thus reducing leakage. Since raising $V_{th}$ also affects performance, the bias can be applied adaptively such that during active mode the reverse bias is small while in standby mode the reverse bias is more negative. Thus, reverse body bias reduces leakage by increasing $V_{th}$ due to decreasing the $\gamma V_{bs}$ term in Equation (10.3).

¹ Multi-Threshold CMOS (MTCMOS) is commonly used as a synonym for power gating, since the most prevalent power gating implementations utilize multiple transistor thresholds. However, it has also been used to refer to the use of non-power gated CMOS circuits designed utilizing multiple transistor thresholds. In this chapter, MTCMOS will be used synonymously with power-gating, while multi-$V_{th}$ denotes the use of multiple transistor thresholds in otherwise conventional circuit design.