WINNING THE POWER STRUGGLE
IN AN UNCERTAIN ERA

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12.1 INTRODUCTION

The growth of process variability in scaled CMOS requires that it is explicitly addressed in the design of high performance and low power ASICs. This growth can be attributed to multiple factors, including the difficulty of manufacturing control, the emergence of new systematic variation-generating mechanisms, and the increase in fundamental atomic-scale randomness – for example, the random placement of dopant atoms in the transistor channel. Scaling also leads to the growth of standby, or leakage power [7]. Importantly, leakage depends exponentially on threshold voltage and gate length of the device. The result is a large spread in leakage power in the presence of process variations.

Recently, considerable research efforts have focused on developing statistical approaches to timing analysis, including the models and algorithms accounting for the impact of delay variability on circuit performance. These techniques concern themselves with eliminating the conservatism introduced by employing traditional worst-case timing models in predicting the timing yield of the circuit. In view of the importance of variability, new methods are needed to evaluate the power-limited parametric yield of integrated circuits and guide the design towards statistically feasible and preferable solutions. This can be achieved through the migration to statistical optimization techniques that account for both power and delay variability.

In this chapter we examine the impact of variability on power, along with the strategies to counter its detrimental effect and improve performance and parametric yield. In Section 12.2 we provide an overview of process
variability trends and discuss their impact on power and parametric yield. Section 12.3 deals with analytical techniques for evaluating circuit parametric yield considering leakage and timing variability. Section 12.4 presents an overview of optimization strategies for yield improvement. In Section 12.5 we discuss in detail, an efficient algorithm that targets power minimization under probabilistically specified timing and power constraints.

12.2 PROCESS VARIABILITY AND ITS IMPACT ON POWER

Several factors contribute to the growth in process variability [2][3][24][34]. While the continued need for more performance necessitates rapid technology scaling, there are severe limitations to our capacity to improve manufacturing tolerances [22]. This is manifested in the rise of such effects as channel length variation due to the optical proximity effect [13][17]; systematic spatial gate length variation due to the aberrations in the stepper lens [38]; and variation in interconnect properties caused by non-uniform rate of chemical-mechanical polishing (CMP) in layout regions of different pattern density [10][39]. Scaling also brings about parameter uncertainty of a fundamental atomic-level nature. This is best exemplified by variability in transistor threshold voltage due to random dopant fluctuations (RDF). As transistors scale, the transistor channel contains fewer dopant atoms whose precise number and location cannot be controlled, while even small fluctuations can impact threshold voltage significantly [8][16][42].

The patterns of variability are also changing: the intra-chip component of variation grows as a percentage of total variability in key process parameters such as channel length and threshold voltage [4][26]. It is this change that is largely responsible for the need to develop new approaches to timing analysis and optimization, as the traditional methods fail in the presence of uncorrelated intra-chip variability.

The increase in leakage power with scaling, and the strong dependence of leakage on highly varying process parameters, raises the importance of statistical leakage and parametric yield modeling. There are several reasons for increased leakage power consumption. Supply voltage scaling requires the reduction in threshold voltage ($V_{th}$) in order to maintain gate overdrive strength. Threshold voltage reduction causes an exponential increase in subthreshold channel leakage current. To make matters worse, aggressive scaling of gate oxide thickness leads to significant gate oxide tunneling current [41].

For transistors in the weak inversion region, the subthreshold current can be expressed as:

$$I_{sub} \propto e^{(V_{gs}-V_{th})/\eta V_{thermal}} (1 - e^{-V_{th} / V_{thermal}})$$  \hspace{1cm} (12.1)