Weak Inversion MOS Varactors for Tunable Integrators

A tunable integrator is the basic building block of a tunable filter. Traditionally, tunability can be accomplished using a MOSFET-C structure with MOS devices replacing resistors; or, using switches and banks of resistors and capacitors for discrete tuning; or, using transconductance-C techniques; or, using a varactor-R structure with varactors replacing capacitors. A MOSFET-C structure typically requires the MOS devices to be in strong inversion, which might not be feasible given the ultra-low supply voltage requirement. Using switches in the signal path would require voltage boosting to turn on the switches, which raises reliability concerns. The design of highly linear tunable transconductors at very low supply voltages is very challenging. We have thus investigated the use of varactor-R techniques. Variable capacitors, along with resistors and low voltage OTAs, enable us to build active-RC circuits at 0.5 V. For this, we propose the use of a weak-inversion MOS capacitor as a three-terminal varactor. The capacitance is between the gate and the combination of drain and source, denoted here as $C_{gs}$, and the tuning voltage is applied at the body, as shown in Fig. 3.1(a). In strong inversion and in accumulation, this capacitance is the oxide capacitance, $C_{ox}$. In depletion, the intrinsic capacitance is zero as there is no inversion layer. From weak to strong inversion through moderate inversion, the intrinsic $C_{gs}$ changes from zero to $C_{ox}$. Changing the body voltage changes the device threshold voltage, $V_T$, and also changes the inversion level of the device. This changes $C_{gs}$ and the device now behaves as a three-terminal varactor.

In this chapter, after a brief theoretical overview in Section 3.1, in Section 3.2, simulation techniques to model the effect of series parasitic resistance are presented and are compared to device measurements. Circuit applications of the varactor are proposed in Section 3.3.

3.1 Brief theoretical overview

The intrinsic gate-source capacitance, $C_{gs}$, of the device in Fig. 3.1(a), with the drain shorted to the source, is defined as:

$$C_{gs} \equiv -\frac{\partial q_G}{\partial V_S} \bigg|_{V_G, V_B \text{ constant}}$$  \hspace{1cm} (3.1)

where $q_G$ is the charge on the gate, and $V_S$, $V_G$, $V_B$ are the voltages at the source/drain, gate and body, respectively, with respect to ground.

The MOSFET gate charge can be expressed in a compact form in terms of the surface potential using a charge-sheet approximation [43, 70]. In an n-channel device with drain and source connected together, assuming uniform charge along the length of the device, this is given as:

$$q_G = C_{ox} (V_{GB} - \psi_S - \phi_{MS})$$  \hspace{1cm} (3.2)

where $C_{ox}$ is the oxide capacitance, $\psi_S$ is the channel surface potential, $\phi_{MS}$ is the work function difference potential. At a given bias voltage, $\psi_S$ can be solved numerically from:

$$V_{GB} = V_{FB} + \psi_S + \gamma \sqrt{\psi_S + \phi_F \left[\psi_S - (2\phi_F + V_{SB})\right]} / \phi_t$$  \hspace{1cm} (3.3)

Here, $\phi_t = kT/q$, $V_{FB}$ is the flat-band voltage, $\phi_F$ is the Fermi-potential, $\gamma = \sqrt{2q\varepsilon_s N_a/C'_{ox}}$ is the body-effect coefficient, $q$ is the charge of an electron, $\varepsilon_s$ is the permittivity of silicon, $N_a$ is the acceptor doping concentration in the channel and $C'_{ox}$ is the oxide capacitance per unit area. $C_{gs}$ can be derived from (3.1) and (3.2), (3.3).

A long-channel nMOS device (15 fingers, each of width 100 $\mu$m, length 20 $\mu$m) was fabricated in a 0.18 $\mu$m triple-well CMOS process, with the body accessible through the p-well and the drain and source shorted together. The normalized gate-source capacitance of this device, for different bias voltages, is shown in Fig. 3.1(b) and 3.1(c). For an operating point for $V_{GS}$ of about 0.25 V, over the range of $V_{GB}$ from -0.1 V to 0.4 V, the capacitance varies by a factor of 4. At an operating point for $V_{GS}$ of 0.15 V, the capacitance varies from 0 to 0.1 $C_{ox}$. For maximum tuning range, the MOS device can be used at a $V_{GS}$ of 0.15 V in this fabrication process.

3.2 Device measurements and modeling

The varactor was measured and characterized using the Agilent 4284A LCR-meter. Fig. 3.2 depicts the measurement setup. The measured effective capacitance, $C_{eff}$ and series resistance, $R_{eff}$ are defined in Fig. 3.3(a). The effective capacitance is shown in Fig. 3.3(b) as a function of $V_{GS}$ for different $V_{GB}$. Due to the lack of a strong inversion layer, there is significant resistance in series with the capacitance.