Chapter 7

Layout-Aware Circuit Sizing

This chapter completes the description and demonstration of the reuse-based design framework presented here. It basically delves into the why and how of including layout geometric information and layout-induced parasitics within the optimization loop of the cell-level sizing process. Outlined in Chapter 2, these sizing techniques, namely geometrically constrained sizing and parasitic-aware sizing, are now the object of the present chapter.

1 INTRODUCTION

The required features for design quality and productivity are multiple. One of them is to ensure that the reused design achieves an effective use of silicon area because, in volume production, the area of the chip is paramount for determining the final production cost. This can be assured by maximizing the layout regularity, optimizing the component aspect ratios, or even by establishing careful floorplanning for the circuit. Another important concern is related to the degradation of performance due to layout-induced parasitics. Such degradation may require time-consuming, unsystematic iterations between layout generation and circuit sizing to improve a design that fails to meet the intended performance specifications.

In this sense, the design reuse flow described in Chapter 2 envisages the application of appropriate techniques to deal with both concerns (see Fig. 1). Parasitic-aware sizing, to include layout-induced parasitics in the circuit sizing process, and geometrically constrained sizing, to include layout geometric information for the layout to meet geometric objectives, both compose the layout-aware circuit sizing methodology that aims at successfully overcoming such concerns. In this chapter, automation of such a methodology is described.
GEOMETRICALLY CONSTRAINED SIZING

At the layout level, the slicing-based template approach explained in Chapter 5 facilitates the creation of fully reusable analog and mixed-signal (AMS) circuit blocks. This further improves fast and efficient reuse of the circuit block and allows incorporation of layout designer’s expertise within the database representing the circuit block as well.

The quality of the eventually produced layout, however, may be suboptimal since the relative placement of the template building blocks on the two-dimensional layout plane (i.e., the floorplan) remains unchanged during the reuse process (either a technology migration or a performance retargeting). To illustrate this point, consider the examples shown in Fig. 2 (for the sake of simplicity, routing wires are not shown). Although the default sizing of the original circuit layout in Fig. 2(a) is rectangular-shaped and the relative area loss\(^1\) is very low, when this circuit is reused resulting, for instance, the layout

\[^1\] Area loss is defined as the portion of the total circuit layout area that is unused, that is, it is not occupied by building block layouts nor routing wires and the process-mandatory spacing layout rules.