Chapter 3

PHASE-LOCKED LOOP FREQUENCY SYNTHESIZERS
Principles, Analyses, and Design

3.1 INTRODUCTION

In this chapter, detailed analyses of PLL frequency synthesizers are treated. Both integer and Δ–Σ-based fractional-N are considered. Open-loop and Closed-loop gain and phase equations are derived and phase noise theory is introduced. Gain and noise contributions of individual subblocks of the synthesizers are detailed. Loop filter design is also included. Together with simulations performed in chapter 4, the derived equations aid the optimum design and implementation of the two presented fractional-N synthesizer chips described in chapters 5 and 6.

3.2 PHASE-LOCKED LOOP FREQUENCY SYNTHESIZER

A PLL frequency synthesizer is a circuit that faithfully follows and reproduces a scaled reference signal over a wide frequency range. A typical frequency synthesizer block diagram is shown in Figure 3-1.

The phase $\Phi_{\text{samp}}$ of a divided-down reference signal, namely sampling signal, is compared to the phase $\Phi_{\text{feed}}$ of the feedback signal obtained by dividing down the oscillator output signal. The mean value of the output signal from the PFD/CP combination is equal to
the phase error between phases \( \phi_{\text{samp}} \) and \( \phi_{\text{feed}} \). When passive loop filter is employed, a CP is used to convert the voltage to current. The CP phase error \( \phi_{\text{CP}} \) then drives the loop filter. Other high-frequency components also present at the output of the CP are removed by the loop filter. The phase error at the output of the filter, \( \phi_{\text{filt}} \) controls the input voltage of the oscillator to obtain the frequency of interest \( f_{\text{out}} \) with a phase \( \phi_{\text{out}} \). A brief description of the PLL subblocks is listed below.

![Figure 3-1. Phase-Locked Loop Frequency Synthesizer](image)

### 3.2.1 Phase-Locked Loop Main Blocks

The main blocks used in the PLL are briefly described below. Detailed description of those blocks is included in the appendices.

#### 3.2.1.1 Phase-Frequency Detector

The PFD [2] compares the divided down reference signal with the divided down feedback signal to generate a signal proportional to the phase error. Several types of frequency detectors are used in PLLs [13]; however, the most commonly used is the PFD as it offers both phase and frequency comparison. A conventional PFD is shown in Figure 3-2.

The timing diagram for this PFD for the case of a reference signal lagging the VCO feedback signal is shown in Figure 3-3. The up and down pulses shown control the source and sink currents that charge or discharge the loop filter capacitor as described below. A detailed description of this PFD as well as other types of PFDs is included in Appendix A.