The increasing demand for high-speed data links for both mobile and wired applications has spawned ever faster communication protocols which require new architectures and circuits to fulfill the performance requirements (speed, error rate) and keep power consumption and cost low enough to be attractive as consumer applications. One such protocol is Digital Subscriber Line (DSL) which is designed to enable transmission data rates in the Mbit/s range while making use of the existing plain old telephone service (POTS) lines originally designed for a bandwidth as small as 7kHz.

The block schematic of a typical DSL transceiver is shown in Fig. 7.1. Most of the signal processing, from modulation/demodulation to raw data input/output is handled by the DSP, so the entire system is flexible and easy to re-configure, assuming the analog components provide enough SNR and bandwidth. The outbound bit streams are fed into the DAC by the DSP. Because the DSL protocols use multicarrier modulation (by splitting the entire bandwidth available in a number of narrow channels), an image rejection filter is used to attenuate the sampled signal’s spectral components at multiples of the sampling frequency (images) so they do not interfere with the other channels. In the case of frequency-division duplexing (FDD) or frequency-division multiplexing (FDM) signals, a band-splitting transmit filter is used (Tx filter). In the case of EC systems there is no Tx filter filter in the transmit (Tx) path. Instead, digital echo cancellers are implemented by the DSP to subtract the Tx signal from the received signal (Rx). Finally, a line driver is used to drive the line impedance which is 100Ω in US and 135Ω in Europe.

The receive path begins with the Rx amplifier (Rx Amp) which is a difference amplifier with programmable gain. An Rx filter is required in FDD or FDM
systems and can also be employed with EC systems if the Tx bandwidth is larger than the Rx bandwidth. The programmable gain amplifier PGA is needed to adapt the input signal range to that of the ADC after the signal is passed through the anti-aliasing filter.

Because DSL systems perform the modulation/demodulation in the digital domain, the ADC and the DAC have to process not only a single, narrowbandwidth channel but the entire communications bandwidth. This is the concept of the "software radio" applied at much lower frequencies than RF communications. Total bandwidth for ADSL, the most popular DSL protocol, is 1.1MHz [43]. But the most aggressive member of the family, VDSL, can extend up to 12MHz bandwidth. On the Rx path this means the ADC should be able to convert a bandwidth in the order of 1 to 10MHz with a resolution which is high enough to guarantee a certain bit error rate (BER), as specified by communication standards. Increasing the resolution of the ADC can simplify the overall system by softening requirements imposed on analog filtering due to increased tolerance to interferers. In the same time, a better use of channel capacity can be obtained by making the channel noise the dominant source of error.

This Chapter describes in detail the design of a high-resolution, broadband $\Sigma\Delta$ ADC. The design starts from a top-level specification extracted from performance requirements of the DSL transceiver chain. From this specification and taking into account technology constraints, an optimal solution is found using the CAD programs covered in Chapter 5. The design is then implemented at transistor-level and, at this level, Spice-like simulations are performed to measure the final power consumption and performance in terms of noise and linearity. In the following Section, the performance requirements of the $\Sigma\Delta$ ADC are calculated from the DSL channel performance. In Section 7.2, an optimal solution is found based on performance, technology constraints and other