6.1 Introduction

The problem of substrate noise coupling on the system level is very hard to attack. As the number of devices in the design increases it becomes difficult to take the entire system netlist to a simulator and simulate the overall system performance. Simulation time and simulator capacity become two major roadblocks in any production worthy design. The interconnect parasitics within blocks and those of the top level routing that connect blocks together adds to the size of the netlist and in many cases causes the simulator to run out of capacity and/or face conversion and runtime issues specially in RF designs where the simulations are based on complex Harmonic balance [54] or periodic steady state algorithms [55]. If we are to add to that the substrate model of the entire system to simulate the noise coupling between major blocks specially in the presence of the digital signal processing block or a high power interfering signal “blocker”, we will be making it harder for the design environment to handle the problem. For such system level validation problems the industry has come with fast spice simulators and behavior level modeling to aid the issue of system level verification, but both have their limitations. First fast spice solvers are transient only based and in an RF chip where inter-modulation and phase noise with and without a blocker are important, it requires very careful simulation setups and fast Fourier transformation to go back and forth between transient and frequency domains and in going back and forth quantization errors are inevitable, in addition to the simulation setups and runtime hurdles. For behavioral modeling it is fairly impossible to model the substrate noise coupling except if you take measurements and fit Si data to the behavioral model, which is too late in the design cycle. Also scalability is another issue in the behavioral modeling. In our design flow the substrate network is selectively added only to critical portions of the system where substrate coupling matters, while the rest of the system remains without such model to achieve the needed compromise between accuracy on one side and capacity and speed on the other side.
6.2 System Level Case Study

Our case study for the substrate noise coupling on the system level can be summarized as follows. The design at hand is a quad band RF front end receiver for cellular application. Figure 6.1 shows the high level block diagram of such receiver [56]. Four LNA’s are present to handle the quad band input signal. A VCO representing the local oscillator “LO” and the LO path, that contains the frequency dividers, feeds a quadrature mixer for frequency down conversion. A filter with an automatic gain control is used to produce the final quadrature signals. A digital controller block receivers a serial interface input and provides control signals to all the blocks on chip. Two versions of this chip were measured, version A and B, and the problem statement is as follows.

Version A was marginally meeting some system specs while failing others, some of its blocks were not meeting the block spec. Version B, the enhanced version, was meeting all the block specs. For the entire system, the carrier to noise ratio $C/N$ of the entire receiver chain in the presence of a strong CW (continuous wave) blocker signal 3 MHz away from the carrier at the high band (1.9 GHz) is failing the spec., (Version A does not have this specific problem). So the goal of this study is to: use the substrate noise coupling design flow developed and calibrated in Chapters 2 and 3 and the design guide developed in chapter four to analyze the VCO and blocker signals coupling through the substrate for the two versions of the chip, and look for discrepancies that may explain the different blocker performance on the two designs, then provide a solution for this problem to pass the system spec.

6.2.1 Background

The phase noise “PN” performance of an LO signal plays a key role for the overall performance of the wireless system by determining how closely channels can be