Chapter 17
Asynchronous On-Line Monitoring of Logical and Temporal Assertions

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Abstract PSL is a standard formal language to specify logical and temporal properties under the form of assertions. This paper presents the synthesis of PSL assertions into asynchronous hardware monitors that can be linked to the circuit under monitoring. The checker synthesis is based on a systematic interconnection of asynchronous primitive monitors corresponding to PSL operators. The asynchronous monitors are implemented with quasi delay insensitive logic which gives reliable and robust monitors in the case of truly asynchronous events, temperature or voltage variations. These monitors are applicable to a wider range of verification tasks such as the communications among globally asynchronous modules or in safe or secure applications.

Keywords PSL, SVA, hardware monitors, asynchronous circuits

17.1 Application Context

New design paradigms are required for large systems on a chip, among which the systematic use of software and hardware “platforms”, and rigorous specification, verification and test methods. In this context, the use of declarative assertions, to specify the expected functional and temporal properties of modules and/or their environment, is recognized as a valuable, time saving technique [12] that can be carried across description levels and serve a wide range of usages. Assertions are useful for specifying constraints for correct IP utilization, the results delivered by IPs, the correct expected design behaviors, etc. As a Boolean property expected to

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be true, an assertion can be evaluated by simulation, emulation or formal verification. An assertion can also be seen as a high level functional specification for a circuit primarily intended for snooping on events over time.

Several formalisms have been developed to ease writing temporal and logical properties, among which SystemVerilog Assertions and PSL are IEEE standards [13, 14]. Synthesizing an asserted property as a monitor, and interconnecting the design and the monitor, is a common technique to design validation and online circuit testing that promises to become increasingly useful for large embedded systems.

The on-going work reported in this paper aims at automatically generating truly asynchronous and synthesizable monitors from PSL assertions, for online checking of circuits in normal operation. Moreover, the monitors can easily be simulated and emulated on a hardware platform. The design debugging on a FPGA board is also an obvious application of our method, with the advantage of permitting full operation speed.

In this context, many applications are foreseen. Some examples are given below:

- Monitoring large systems built from synchronous IP’s: one difficulty in debugging “globally asynchronous locally synchronous” systems is the correctness of communications. Asynchronous monitors are needed to pinpoint erroneous transactions between modules that belong to different clock domains.
- Monitoring inherently asynchronous events, guaranteeing that an appropriate response is given, irrespective of the events delay.
- Safely monitoring circuits in harsh environments thanks to the intrinsic robustness of asynchronous logic.
- Monitoring secure chips, such as cryptoprocessors, in order to detect side-channel attacks using fault injections.

17.2 State of Art

FOCS from IBM [1, 6] was, to our knowledge, the first tool to automate the generation of register-transfer level (RTL) monitors from PSL, producing VHDL or Verilog code that can be linked to the design at hand for checking on a clock cycle basis. Although primarily intended for on-line simulation, including mixed signal simulation by other parties [2], monitors produced by FOCS are synthesizable, and can be fed to a model checker. The principles for building syntax directed monitors for clock synchronized “foundation language” PSL expression [7] and SERE’s [9, 15] have been disclosed with a particular emphasis on debugging feature [8, 15]. A more formal automata theoretic construction of monitors, the so-called “temporal testers”, are also built in a compositional way [17]. Cimatti et al. [10] propose another modular encoding to turn PSL properties into nondeterministic Büchi automata. Other tools are now provided by the main CAD companies, that interface