Modern IC designs have reached unparalleled levels of overall complexity, and thorough verification is becoming more difficult. Furthermore, the verification problem is exacerbated by the highly competitive market which requires shorter time-to-market. As a result, design errors are more likely to escape verification in the early stage of the design flow and are found after layout has been finished; or even worse, after the chip has been taped-out. Needless to say, these errors must be fixed before the IC can reach the market. Fixing such errors is often costly, especially when the chip has been taped-out. The key to reduce this cost is to preserve as much previous effort spent on the design as possible. In this chapter we present error-repair techniques that support the post-silicon debugging methodology described in Section 4.4. However, these techniques can be applied to pre-silicon layout optimization or error repair as well.

As mentioned in Section 2.4, design errors that occur post-silicon can be functional or electrical, and various physical synthesis techniques may be used to fix such errors. However, there is no metric to measure the impact of a physical synthesis technique on the layout. In this chapter, we first define and explore the concepts of physical safeness and logical soundness to measure such an impact. We observe from this analysis that most existing physical synthesis techniques do not allow post-silicon metal fix, and those support metal fix have limited error-repair capabilities. Therefore, we propose a SafeResynth technique that is more powerful yet has little impact on a layout. The next section then describes how SafeResynth can be applied to repair post-silicon electrical errors. In addition, the section also illustrates our new functional and electrical error repair techniques. This chapter concludes with experimental results and a brief summary.
11.1 Physical Safeness and Logical Soundness

The concept of physical safeness is used to describe the impact of an optimization technique on the placement of a circuit. Physically safe techniques only allow legal changes to a given placement; therefore, accurate analysis such as timing and congestion can be performed. Such changes are safe because they can be rejected immediately if the layout is not improved. On the other hand, unsafe techniques allow changes that produce a temporarily illegal placement. As a result, their evaluation is delayed, and it is not possible to reliably decide if the change can be accepted or must be rejected until later. Therefore, the average quality of unsafe changes may be worse than that of accepted safe changes. In addition, other physical parameters, such as wirelength or via count, may be impacted by unsafe transformations.

Similar to physical safeness, logical soundness is used to describe the perturbation to the logic made by the optimization techniques. Techniques that do not change the logic usually do not require verification. Examples for this type of optimization include gate sizing and buffer insertion. Techniques that change the logic of the circuit may require verification to ensure their correctness. For example, optimizations based on reconnecting wires require verification because any bug in the optimization process may change the circuit’s behavior. Since local changes to combinational logic can be verified easily using equivalence checking, they are considered logically sound. However, small changes to sequential logic often have global implications and are much more difficult to verify, therefore we do not classify them as logically sound techniques. These techniques include the insertion of clocked repeaters and the use of retiming.

11.1.1 Physically Safe Techniques

Symmetry-based rewiring is one of the few physical synthesis techniques that is physically safe in nature. As described in Chapter 7, it exploits symmetries in logic functions, looking for pin reconnections that improve the optimization objective. For example, the inputs to an AND gate can be swapped without changing its logic function. Since only wiring is changed in this technique, the placement is always preserved. An example of symmetry-based rewiring is given in Figure 11.1(a).

The advantage of physically safe techniques is that the effects of any change are immediately measurable, therefore the change can be accepted or rejected reliably. As a result, circuit parameters will not deteriorate after optimization and no timing convergence problem will occur. However, the improvement gained from these techniques is often limited because they cannot aggressively modify the logic or use larger-scale optimizations. For example, in [32] timing improvement measured before routing is typically less than 10%.