Chapter 1
Introduction of On-Chip Crosstalk Avoidance

1.1 Challenges in Deep Submicron Processes

The advancement of very large scale integration (VLSI) technologies has been following Moore’s law for the past several decades: the number of transistors on an integrated circuit is doubling every two years [4] and the channel length is scaling at the rate of 0.7/3 years [41, 68]. It was not long ago when VLSI design marched into the realm of Deep Submicron (DSM) processes, where the minimum feature size is well below 1 μm. These advanced processes enable designers to implement faster, bigger and more complex designs. With the increase in complexity, System on Chip (SoC), Network on Chip (NoC) and Chip-level Multiprocessing (CMP) based products are now readily available commercially.

In the meanwhile, however, DSM technologies also present new challenges to designers on many different fronts such as (i) scale and complexity of design, verification and test; (ii) circuit modeling and (iii) processing and manufacturability. Innovative approaches are needed at both the system level and the chip level to address these challenges and mitigate the negative effects they bring.

Some major challenges in DSM technologies include design productivity, manufacturability, power consumption, dissipation and interconnect delay [68, 93]. High design cost and long turn-around time are often caused by the growth in design complexity. A high design complexity results from a growth in transistor count and speed, demand for increasing functionality, low cost requirements, short time-to-market and the increasing integration of embedded analog circuits and memories. Poor manufacturability is often a direct result of reduction in feature size. As the feature size gets smaller, the design becomes very sensitive to process variation, which greatly affects yield, reliability and testability. To address these issues, new design flows and methodologies are implemented to improve the efficiency of the designs. IC foundries are adding more design rules to improve the design robustness.

For many high density, high speed DSM designs, power consumption is a major concern. Increasing transistor counts, chip speed, and greater device leakage are driving up both dynamic and static power consumption. For example, increased leakage currents have become a significant contributor to the overall power dissipation of Complimentary Metal Oxide Semiconductor (CMOS) designs beyond...
90 nm. Consequently, the identification, modeling and control of different leakage components is an important requirement, especially for low power applications. The reduction in leakage currents can be achieved using both process and circuit level techniques. At the process level, leakage reduction can be achieved by controlling the device dimensions (channel length, oxide thickness, junction depth, etc) and doping profile of transistors. At the circuit level, leakage control can be achieved by transistor stacking, use of multiple $V_T$ or dynamic $V_T$ devices etc. The high power consumption density also make the heat dissipation critical and often requires advanced packaging.

A critical challenge which we will address in Part I is the performance degradation caused by increased on-chip interconnect delays in advanced processes. As a result of aggressive device scaling, gate delays are reducing rapidly. However, interconnect delays remain unchanged or are reducing at a much slower rate. Therefore the performance of bus based interconnects has become the bottleneck to overall system performance. In many large designs (e.g. SoC, NoC and CMP designs) where long and wide global busses are used, interconnect delays often dominate logic delays. For example, in a 90 nm process, the typical gate delay is $\sim 30$ ps. The interconnect delay, however, can easily be a few nanoseconds in a moderate sized chip.

### 1.2 Overview of On-Chip Crosstalk Avoidance

Once negligible, capacitive crosstalk has become a major determinant of the total power consumption and delay of on-chip busses. Figure 1.1 illustrates a simplified on-chip bus model with crosstalk. In the figure, $C_L$ denotes the *load capacitance*, which includes the receiver gate capacitance and also the parasitic wire-to-substrate parasitic capacitance. $C_I$ is the *inter-wire coupling capacitance* between adjacent signal lines of the bus. In practice, this bus structure is typically modeled as a