Chapter 13
Bus Expansion Encoder

When determining the performance of an off-chip bus, the worst-case noise magnitude must be considered in order to ensure a robust digital system. Chapter 11 presented an analytical model to predict the performance of an off-chip bus using the assumption that each of the noise sources within the package contributes its worst-case noise. Each source of noise within the package (Sect. 8.2) had a particular set of data sequences that resulted in the worst-case noise. This set of sequences dictates the highest performance that the package can achieve. The sequences that result in noise (from any noise source) above a certain magnitude can be avoided by designing an encoder which eliminates such sequences. This increases the performance of the package. By inserting this encoder in the signal path on the IC, it ensures that the off-chip data is encoded before traversing the package interconnect. In this way, data sequences which result in noise above a specified limit can be avoided and the bus performance can be increased.

The encoder is constructed to remove any bus sequence which results in a noise event (regardless of the noise source) above a user-specified value. Experimental results demonstrate that this methodology improves the overall performance of the bus even after considering the overhead of the encoder circuit.

The technique maps each element in the original set of on-chip data sequences to an element in an alternate set of sequences (whose noise is bounded by the user-specified limit). Since the alternate set of sequences has a width greater than the width of the original bus, we refer to the resulting circuit as a bus expansion encoder. The construction of the encoder/decoder utilizes an implicit, Reduced Ordered Binary Decision Diagram (ROBDD). If it is desired that the noise due to one or more noise sources (described in Sect. 8.2) should be reduced, the method can be employed.

13.1 Constraint Equations

The first step in creating the bus expansion encoder is to create a set of constraint equations. The constraint equations are written so that arbitrary transitions can be evaluated for noise limit violations. When a transition is evaluated using the constraint equations and violates one of the user-defined noise limits, the transition is flagged as illegal and is removed from the set of data sequences that are allowed to be
driven through the package interconnect. Each of the possible off-chip transitions are evaluated against each of the constraint equations. The enumeration of the off-chip transitions is done implicitly, so as to increase the applicability of the technique. After the evaluation is complete, a subset of legal transitions remain which are used in the construction of the encoder.

13.1 Supply Bounce Constraints

When a pin $i$ in segment $j$ is a $V_{DD}$ pin, it is required that the bounce magnitude due to the electrical parasitics in the package must not exceed the user-defined noise limit $P_{supply}$. When the pin under evaluation is a $V_{DD}$ pin, a constraint equation is written to determine if any transitions that occur on the bus segment will result in a violation of $P_{supply}$. The constraint equation takes into account the voltage noise due to the self-inductance of the $V_{DD}$ pin in addition to any mutual inductive or capacitive coupling that occurs due to switching signals in adjacent pins. By multiplying the coupling magnitude by the transition value $v_{ij}$ (which can be 0, 1, or $-1$), the magnitude and sign of the induced noise value is accounted for. This handles the situation for a static pin a static signal pin ($v_{ij} = 0$) which has no effect on the noise on the supply pin.

The following constraint equation is written for any pin $i$ within a bus segment $j$ that is used as a $V_{DD}$ pin, and is being evaluated for a supply bounce violation:

\[
\text{\textbullet } v_{ij} = V_{DD} \Rightarrow P_{\text{supply}} \cdot V_{DD} \geq \left( \frac{d}{dt} \right) \left[ (L_{11} \cdot (N_{1}) + \sum_{k=-p_{L}}^{k=p_{L}} [(M_{1})_{i}^{k}] \right] \\
\times \left( v_{i+k} \right) + \sum_{k=-p_{C}}^{k=p_{C}} \left[ \left( \frac{C_{1}^{k}}{(0.8)} \cdot Z_{2} \right) \cdot \left( v_{i+k} \right) \right]
\]

When a pin $i$ in segment $j$ is a $V_{SS}$ pin it is required that the bounce magnitude due to the electrical parasitics in the package must not exceed the user-defined noise limit $P_{gnd}$. When the pin under evaluation is a $V_{SS}$ pin, a constraint equation is written to determine if any transitions that occur on the bus segment will result in a violation of $P_{gnd}$. The following constraint equation is written for any pin $i$ within a bus segment $j$ that is used as a $V_{SS}$ pin, and is being evaluated for a ground bounce violation:

\[
\text{\textbullet } v_{ij} = V_{SS} \Rightarrow P_{\text{gnd}} \cdot V_{DD} \geq \left( \frac{d}{dt} \right) \left[ (L_{11} \cdot (N_{-1}) + \sum_{k=-p_{L}}^{k=p_{L}} [(M_{1})_{i}^{k}] \right] \\
\times \left( v_{i+k} \right) + \sum_{k=-p_{C}}^{k=p_{C}} \left[ \left( \frac{C_{1}^{k}}{(0.8)} \cdot Z_{2} \right) \cdot \left( v_{i+k} \right) \right]
\]

13.1.2 Signal Coupling Constraints

13.1.2.1 Glitch Magnitude Constraints

When a pin $i$ in segment $j$ is a signal pin, it is required that the coupled voltage onto that pin does not exceed any of the user-defined noise limits for signal coupling. If the signal pin is static ($v_{ij} = 0$), then the glitch magnitude onto the victim pin must not exceed $P_{0}$. As in the constraint equations for supply bounce, the magnitude of the coupling contribution of any neighboring pin is multiplied by the transition value $v$.