Multi-Layer Interdigitated Power Distribution Networks

An interdigitated P/G distribution network structure is the most common structure in high complexity integrated circuits. Typically, a few wide lines are replaced by a large number of narrow lines to reduce the effects of inductance [230], [231]. Different P/G structures have been compared in [70], where the interdigitated structure is shown to achieve the greatest reduction in inductance.

An interdigitated P/G distribution structure is typically located on several metal layers. Each layer consists of interdigitated power and ground wires, where the direction of the wires is perpendicular to the direction of the wires in the previous layer, as depicted in Fig. 25.1. With advancements in technology, additional metal layers are provided [369], permitting the dedication of several metal layers to the P/G network. Due to electromigration, the maximum current is limited; therefore, a larger number of metal layers passes higher current to the microelectronic system while not surpassing any electromigration constraints.

The need for efficient P/G networks has been recognized, and several algorithms and techniques to optimize the P/G distribution network have been reported [204], [370]. A routing tool for standard cell circuits to efficiently supply and distribute power has been proposed in [371]. A typical high complexity IC however includes a variety of circuits, therefore, routing the supply network within a standard cell design flow can produce an ineffective network. To overcome this issue, several algorithms based on different optimization strategies have been developed [372], [373]; however, only the package inductance is considered in [373], neglecting the on-chip inductance. An algorithm based on partitioning the power/ground network into smaller sections is proposed in [374], where $IR$ voltage drops are considered. With more
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advanced packaging techniques (such as flip-chip), the on-chip inductive noise \( L \frac{dI}{dt} \) is also important [126], [215]. To consider on-chip inductance in power/ground networks, a technique to simplify the mesh model of an \( RLC \) power/ground network is proposed [375], assuming the loads are treated as identical current sources. The significance of the on-chip inductance within paired and interdigitated power/ground network structures is described in [376], where the inductance is treated as a local effect. In [268], the inductance model considers the mutual inductance between close and distant power/ground wires in interdigitated structures. Based on this model, a closed-form expression characterizing an interdigitated P/G network structure is described, permitting the optimal width of a power/ground network that minimizes the network impedance to be determined. Based on the optimum width of the power/ground lines, a methodology is described in this chapter to minimize the impedance under current density constraints for a multi-layer metal system.

**Fig. 25.1.** Global interdigitated P/G distribution structure. The darker and lighter lines represent, respectively, the power and ground lines.

This chapter is organized as follows. A closed-form expression describing the minimum impedance for a single metal layer is presented in Section 25.1. In Section 25.2, several methods to lower the current density across multiple metal layers are described. Two different approaches are suggested. The tradeoff between the impedance of a P/G network and the current density is presented in Section 25.3. This chapter is summarized in Section 25.4.