INTRODUCTION

The translinear principle has become quite familiar to IC designers during the past twenty years. Originally conceived within the narrow framework of bipolar, wideband, fixed- and variable-gain current-mode amplifiers employing closed loops of junctions [1,2]—now called TL cells, in which input and output signals and biases are all in pure current form—the scope of the concept has gradually broadened to include any circuit in which the essential function depends directly on a precise exponential relationship existing between the current at one terminal of a suitably-biased three-terminal active device and the voltage applied across the remaining two terminals. A translinear cell not including any directly closed loops has more recently [3] been called a translinear network (TN).

For the BJT, this key relationship exists between the collector current \( I_C \) and the base-emitter forward-bias voltage \( V_{BE} \). It will be apparent that SiGe heterojunction bipolar transistors (HBTs) exhibit the same essential exponential behaviour and therefore can be used in all translinear applications with little if any modification to the theory. The absolute value of the band-gap voltage—hence, the \( I_S(T) \)—does not appear in the final equations of TL circuits, nor in many TN circuits; thus, GaAs HBTs (having a \( V_{BE} \) of over a volt) may be used, or even pure-germanium transistors (usefully having a \( V_{BE} \) of about half that of silicon), if such might ever be fabricated in monolithic form.

This idea has more recently been applied to MOS devices operating in the sub-threshold (weak inversion) domain [4]. But the original formulation of the principle, since expounded at greater length by Seevinck [5], cannot be applied to translinear-loop cells using enhancement-mode MOS transistors operating in strong inversion, because, at least according to simple theories, the channel current \( I_{DS} \) of an MOS transistor bears a quadratic relationship to the gate-source voltage. Consequently, Seevinck and Wiegerink have proposed an alternative formulation [6] of the ‘translinear idea’, based on the observation that, in contrast to the BJT, which (for a \( V_{CE} \) greater than about 200mV) exhibits a linear relationship between the transconductance \( g_m = \partial I_C / \partial V_{BE} \) and the collector current, MOS devices in strong inversion (and with \( V_{DS} > V_{GS} \)) exhibit this linear relationship between the transconductance \( g_m = \partial I_{DS} / \partial V_{GS} \) and the excess voltage \( V_{GS} \) above the threshold voltage, \( V_{TH} \).
This extension of the original principle has been called 'MOS translinear', or MTL. However, the mathematical relationships are very different, and are much less tractable than the simple 'repeated product' form of the translinear-loop principle based on exponential junction behaviour. Furthermore, the 'quadratic-\(I_{DS}\) assumption is only an approximation, even for long-channel devices, with serious non-idealities in practice, due to channel-length modulation below 1\(\mu\)m, as well as back-gate effects; these are rarely addressed with adequate realism in the literature. In fact, for modern sub-micron MOS transistors, it is the \(I_{DS}\)—not the \(g_m\)—which is an almost linear function of \(V_{DS}\) above \(V_{TH}\), and the cell behaviour errs very significantly from that predicted by 'MTL' theory.

To avoid going beyond the spirit of the original definition of 'translinear', and risking ambiguity about the intended meaning and application of the term in MOS applications, its use without an adjectival qualifier should be reserved for those cells invoking exponential device behaviour, in recognition of long-standing and familiar usage. The strong-inversion idealization should be termed voltage-translinear, or VTL, since the proposed acronym MTL, when read as 'MOS-translinear', could refer to either the VTL mode or to classical translinear operation (either TL or TN) using MOS transistors in subthreshold.

It is likely that the increasing utilization of CMOS in analog applications will gradually soften the dependence on translinear techniques, which have yielded an impressive portfolio of bipolar integrated circuits, and continue to be of value, either in new applications (or the rediscovery) of classical cell topologies, or in more subtle ways. On the other hand, little use can be made of the idea in the CMOS domain. A noteworthy exception is the implementation neural networks [7,8], using MOS devices at very low currents, where their bipolar-like behaviour can be exploited; a new development in this field is the use of floating-gate cells [9] to perform summing of exponential arguments, hence multiplication, in an otherwise classical translinear modality. Such applications generally place very modest demands on accuracy, so considerable deviation from the presumed device 'law' is of little consequence. Similarly, modest accuracy requirements allow VTL cells to be employed in specialized non-demanding applications [10].

1 EARLY TRANSLINEAR CELLS

The basic idea of a translinear circuit was conceived by the author in 1967, in the context of high-bandwidth (500MHz) electronically-variable gain cells, for use in oscilloscope vertical amplifiers at Tektronix Inc. Out of this initial work came many developments, one of which was a monolithic doubly-balanced modulator (or mixer, a nonlinear multiplier), which was then linearized by the addition of another pair of BJTs to realize a wideband four-quadrant analog multiplier, reported in February 1968 at one of the earliest International Solid-State Circuits Conferences in Philadelphia [1] and later described in full detail in two seminal papers [11,12] which anticipated many of the translinear circuits that would later be turned into commercial products, including high-accuracy and wideband multipliers [13,14], RMS-DC converters [15], an analog array processor [16], as well as a variety of other interesting and useful nonlinear