Chapter 6

Wi-FLIP: A Low-power Vision-enabled WSN Node

Wi-FLIP is the system resulting from the integration of FLIP-Q, the prototype vision chip just described, and Imote2, the commercial WSN platform briefly commented in Sect. 2.1. This platform gathers certain features that make it appropriate for such integration. First of all, it contains a digital processor whose frequency can vary from 13 MHz up to 416 MHz with dynamic voltage scaling. This means an enormous flexibility when it comes to adjust the power consumption of the system in function of the timing requirements of the artificial vision application considered. Additionally, the amount of memory available, 256 kB SRAM, 32 MB SDRAM and 32 MB FLASH, suffices for image processing algorithms of low-medium complexity, suitable for WSN environments. Finally, thanks to its dense pinout, Imote2 can carry out the control of FLIP-Q as well as retrieve the simplified scene representations it generates.

6.1 Imote2: System Description

The top and bottom views of Imote2 (model IPR2400) (Imote2, MEMSIC) together with a block diagram containing its different modules are depicted in Fig. 6.1. The 32-bit ARM5 PXA271 XScale® processor (PXA271, Marvell) constitutes the system core. Its most remarkable feature is the above mentioned programmability of the clock frequency in conjunction with dynamic voltage scaling. A number of different low power modes is available. TinyOS (Levis and Gay 2009), an event-driven operating system tailored for low-power wireless devices, runs on this processor. An 802.15.4 radio (CC2420, Texas Instr.) with an on-board antenna is also integrated. The CC2420 radio transceiver supports a 250 kbps data rate with sixteen channels in the 2.4 GHz band. The antenna enables a nominal range of about 30 m. For longer ranges, a SMA connector can be soldered directly to the board to connect an external antenna. Two interfaces for external interconnection are provided: a so-called “basic sensor board” interface, consisting of two connectors on the top side of the board, and an “advanced sensor board” interface, consisting of two high density connectors on the bottom side of the board. Through these interfaces, a wide set of standard I/O options is delivered. In our case, the most interesting aspect is the great
Fig. 6.1 Top and bottom view of *Imote2* along with its block diagram

number of GPIOs available. To supply the processor with all the required voltage domains, a Power Management Integrated Circuit (PMIC) is included. This PMIC supplies 9 voltage domains to the processor in addition to the dynamic voltage scaling capability. It also includes a battery charging option through USB and battery voltage monitoring. *Imote2* was designed to support primary and rechargeable batteries through an attachable battery board (IBB2400, MEMSIC), as well as to being powered via USB.

Table 6.1 summarizes the main operating parameters of *Imote2* provided by the vendor. The figures related to power consumption have been confirmed during the experimental tests of *Wi-FLIP*. They correspond to a basic configuration where the minimum possible number of PXA271’s modules are active. These figures are given in terms of current consumption, what results very useful to rapidly estimate the lifetime of the batteries. Note that, for the configuration where the PXA271 processor works at minimum clock speed, i.e. 13 MHz, the maximum current consumed by our prototype, 1.7 mA, represents only the 5.2% of the whole system current consumption, 32.7 mA. This percentage gets even lower as the clock speed increases.

### 6.2 Interconnection Plan

The *FLIPQ*-to-*Imote2* interconnection has been carefully realized according to the number of PXA271’s GPIOs available. Specifically, there are 34 GPIOs which can be accessed through the 40-pin connector of the “advanced sensor board” interface depicted in Fig. 6.2. The interconnection plan is showed in Table 6.2. Only the strictly necessary logic to enable the processing primitives implemented by the *FLIP-Q*