18.1 Introduction

In the last three decades, many innovative microelectronics packaging and interconnection-related technologies, such as tape automated bonding (TAB), flip chip, multi-chip modules (MCMs), and ball grid arrays (BGAs), have been developed, applied, and demonstrated in a variety of electronic products. The demand for high-density, high-performance, high-function, portable consumer electronics continues almost undiminished. The ever-increasing demand for product performance, versatility, and miniaturization, resulted in significant advances in semiconductor device power, performance and pin count. These, in turn, have imposed significant challenges upon electronic companies to provide even more compact, cost-effective, and reliable products [1,2].

18.1.1 Background

Chip scale packaging (CSP) is a relatively new packaging technology innovation that was first introduced to industry in approximately 1993. The chip-scale concept was simultaneously proposed by Junichi Kasai of Fujitsu and Gen Mukarami of Hitachi Cable [3] and was demonstrated by Mitsubishi Electric about ten years ago.

18.1.2 Utilization

CSPs can be viewed as an enabling technology for near-term miniaturization for the high-function mobile information processing industry. CSPs are used in a variety of applications where I/O requirements range from 20-289 I/O, encompassing global positioning systems (GPS), flash memory, SDRAM, RDRAM, digital signal processors (DSP), and some logic and ASIC devices. Figure 18-1 indicates that nearly a 90% package area reduction is attainable by migrating from a quad flat pack to a bare die. The technology is believed to be a low-cost alternative to flip-chip attach (FCA) since it may not require underfilling for many applications.

Chip scale packaging has become a very important single-chip packaging technology because an integrated circuit (IC) device can be packaged in a format that is much lighter,
thinner, and smaller than conventional IC packages (Fig. 18-1). Several, system manufacturers have adopted CSPs for use in portable products such as notebook computers, cellular phones, and digital camcorders [4–10].

18.1.3 CSP vs. DCA/Conventional Packages

CSPs offer an alternative or an intermediate solution to flip chip or direct chip attach technology by enabling the use of current surface mount assembly equipment. In a number of applications an underfill is not required for reliable performance. In fact, the underfill process is a major drawback of direct chip attach (DCA, i.e., flip chip on board) technology. In general, CSPs exhibit improved electrical performance over other packages, and are ideally suited for portable products where size, weight, and robustness are important considerations. A footprint comparison between various BGA and CSP packages, and flip-chip dice is shown in Fig. 18-2, where the bottom sides of the packages are depicted.

The solder balls on area array CSPs collapse to a stand-off height approximately 60 percent of the original ball diameter during solder reflow attachment. Full arrays with selectively removed solder balls and perimeter arrays are typical. Ribbon bonding connects circuitry on a polymer interposer to a die in some designs. While the definition of CSP seems to emphasize the size, the design