21.1 Introduction

The use of product connectors has mainly involved high-end applications. Electronic modules normally represent a function, and one or more multichip modules typically are combined on a card or board. It is important that some or all the individual modules be easily separable to permit testing, diagnostics and field repair, and that the separable connections not functionally degrade the electrical signals [1]. The intent is to preserve the value of a board and its attached components while having the capability to make repairs or upgrades through component exchanges throughout the lifetime of a part. Several early area-array “compression connection” concepts were reported in the mid 1980s/early 1990s that recognized that a disassembly design must also be capable of high I/O density to accommodate ever increasing I/O counts (i.e., extendible to decreasing pitches). Knight and Winkler [2] described an array of BeCu spring contacts overplated with Ni/Au attached to a PWB on a 0.100 x 0.150 inch interstitial grid. The spring elements make contact with pads (i.e., LGA) on the bottom side of a module. M. Kirkman [3] described a form factor most often utilized today: an array of connector elements held in a dielectric housing, often referred to as an interposer as it is positioned between a module and mating PWB site. When the connector elements are compressed they make intimate contact with both chip carrier and board pads to provide a low-ohmic contact. Product connectors allow replacements to be made in the field, and in some cases by users themselves, thus must be virtually foolproof and not require special tools. The exchange must be made with no adverse effects on functionality and reliability.

21.1.1 Pins

Plug-compatible pinned modules have been utilized in the past as a quick disconnect method. Pinned solutions will become increasingly less acceptable for high-performance, high-I/O applications. Processing and material costs are substantial in consideration of the carrier pads, braze, pins, connector, housing, etc. requirements. More importantly, however, the long pin length and associated connector results in a very high inductance. The optimum power I/O configuration is a thick, short conductor, whereas signal
I/Os require a high density capability, but low current, interspersed alternately with ground to minimize crosstalk and noise [4]. Although a pinned system could be scaled down from the standard 0.100-in. pitch, it is questionable how far below a 0.050-in. pitch this reduction could reasonably be extended to be either electrically or mechanically viable [5].

21.1.2 Migration to Cost Performance

As die sizes, I/O counts and corresponding component sizes increase, connectors will also migrate into some segments of the cost-performance arena with emphasis on low cost and portability (i.e., low weight, small size). In some cases, similar to high-end applications, it is cost prohibitive to discard the card when making a component upgrade, but in most instances the key driver will be predicated on reliability issues. That is, as component footprints become even larger owing to greatly increased I/O requirements, connectors will provide the mechanism to relieve strain generated as a result of the CTE mismatch between ceramic chip carriers and organic cards/boards.

21.1.3 This Chapter

This chapter discusses the differences between test/burn-in and production connectors and their requirements. The stresses that are imposed during actuation and the effect of such factors as: chip-carrier modulus and thickness, die size, seal-band materials, thermal compound materials, chip-carrier/interposer planarity, spring stiffness, etc. are described as well. Various generic product connector configurations and representative commercially-available systems are also discussed. Minimum acceptability tests typically conducted on product connector assemblies and the general results are also described in this chapter. Finally, an insight to the enhancements which are reasonably anticipated in this rapidly emerging technology is presented.

21.2 Generic BGA/LGA Connector Assemblies

21.2.1 Land Grid Array (LGA)

21.2.1.1 Chip carrier and board pads A land grid array connector assembly (Fig. 21-1) typically consists of a ceramic chip carrier fabricated similar to CBGA and CCGA carriers up to the point of ball and column attach respectively. At this point for LGA, the I/O pads are typically over plated with 80 to 100 micro-in Ni and 30 micro-in Au (electroless or electrolytic). Card pads at LGA sites are also over plated with a similar thickness of Ni and Au. In the past, selectively plating card sites was a significant cost adder, but not so now because LGA has become a mainstream technology.

Fig. 21-1 Schematic illustrating the elements that comprise a land grid array (LGA) connector system.