23.1 Introduction

Emerging chip scale packages (CSPs) and miniature versions of ball grid arrays (BGAs), are competing with bare die flip chip assemblies. CSP is an important miniature electronic package technology utilizing low pin counts, without the attendant handling and processing problems of low peripheral leaded packages such as thin small outline packages (TSOPs) and high-I/O (input/output) quad flat packages (QFPs). Advantages include self-alignment capability during assembly reflow process and better lead (ball) rigidity. Reliability data and inspection techniques are needed for CSP acceptance especially for high-reliability applications.

23.1.1 CSP Evolution

Although the expression “CSP” is widely used in microelectronics industry by both suppliers and users, its definition evolved as the technology matured. At the start of the package’s introduction into the market, a very precise definition was adopted by a group of industry experts as a package that is up to 1.2 times larger than the edge length or 1.5 times the area of the die. Soon, it became apparent that suppliers were using the term CSP to promote a miniature version of a previous package. A rapid transition to a much smaller size was difficult for both package suppliers and end users. Suppliers had difficulty building the packages whereas users had difficulties accommodating the need for the new microvia printed circuit board (PWB), mainly because of routing requirements and the increased cost. Other issues for accepting the “interim definition” by industry included lack of maturity in assembly and infrastructure. For example, the use of pitches other than 0.5 mm, including 0.75 and 0.65 mm, was aimed at using a standard PWB design to avoid the increased cost of microvias.

23.1.1.1 Die shrinkage The “expert definition” undermines a key purpose of chip scale packages, allowing for die shrinkage. If die shrinkage is acceptable for the package to retain the footprint, then a decrease in die size for the same CSP results in not conforming to the definition of a CSP. Therefore, in reality, CSPs are miniature new packages that industry is starting to implement, and there are many unresolved technical issues associated with their implementation.

23.1.1.2 Unresolved issues Technical issues themselves also change as packages mature. For example, in early 1997, packages
with a 1-mm pitch and lower were the domi-
nant CSPs, whereas in early 1998 packages
with 0.8-mm and lower became the norm for
CSPs. New issues must be addressed includ-
ing the use of flip-chip rather than wire-bond
die in CSPs. Flip-chip solder joint failures
within CSPs is a potential new failure me-
chanism that needs to be considered.

23.1.2 Implementation Challenges

The JPL-led CSP consortia of enterprises
representing government agencies and pri-
ivate companies joined together to pool in-
kind resources for developing a quality and
reliability data base for chip scale pack-
ages (CSPs) based on a variety of projects.
During the course of the JPL-led consortia,
test vehicles [1] were defined, and numerous
challenges identified. The first test vehi-
cle emerged late in 1996, when few pack-
ages were available for evaluation, and an-
other in 1998, when approximately fifty types
were available. Although the rapid growth
of CSPs has eased package availability, is-
sues of their implementation, especially for
high-reliability applications, requires the es-
tablishment of an assurance for quality and
confidence in reliability in addition to the
necessary infrastructure.

The following section discusses the key
challenges for package and PWB design, as-
sembly of test vehicles, and environmental or
stress test results for CSPs and assemblies.

23.1.2.1 Lack of test vehicle/test data
CSP daisy chain test vehicle availability for
attachment reliability characterization was
an early issue (1997). Although there were
numerous papers covering a wide range of
CSPs in the literature, most packages were
in an early development stage and lacked
reliability information. Assembly reliability
data were even rarer because most pack-
ages were only available as prototypes which
did not necessarily simulate subsequent pro-
duction versions. Long delivery delays were
the norm (6 months or more) often with the
supplier making last moment modifications.
Although many suppliers promoted their
packages and package reliability, there was
a general unwillingness by suppliers to offer
their packages for independent evaluations.
In this period, lack of delivery clearly indi-
cated package suppliers were struggling to
build CSPs especially with a 0.5 mm pitch
and high I/O counts. Therefore, a CSP with
275 I/Os become the maximum by default.

Initially CSPs were generally available
with pitches of 0.8 mm, and then a few high-
I/O CSPs become available with a 0.5 mm
pitch, indicating the industry was progres-
sively becoming more comfortable with
tighter pitches with higher I/O counts.

23.1.2.2 Lack of design guidelines Ini-
itially, guidelines and standards were not
available for various aspects of CSP such as
package daisy-chain information, mechanical
drawing data, etc. The majority of packages
were hard metric, however, the few pitches
based on the English system caused dimen-
sional errors when converting between sys-
tems. There was lack of design information
to achieve optimum properties; as a rule of
thumb, CSP pads were assumed to be the
same as PWB pads for design purposes.

23.1.2.3 Need for microvia PWB A
standard PWB design can be used for low
I/O situations, but build-up (microvia) board
technology is required for high I/O count
CSPs. For daisy-chain packages, it is possible
to accommodate high I/O counts on a stan-
dard board. New board design guidelines are
needed, especially for build-up (microvia)
configurations.

23.1.2.4 I/O limitation Typically the
package I/O count is low, although higher I/O
counts (~500) are available to meet specific
application requirements. Mixtures of con-
vventional surface mount packages including,
TSOP, flip-chip die, BGAs, standard and fine
pitch BGAs, and CSPs on a board present
another design and assembly challenge.

23.1.3 Reliability Scope

This chapter reviews the many factors that
affect interconnect reliability of emerging