Area Array Leverages: Why and How to Choose a Package

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25.1 Introduction

Performance is an attribute that defines how well a given requirement is satisfied and is predicated on priority so may depend upon one or a multiplicity of factors. Among those most often considered in microelectronic packaging are thermal and electrical characteristics, size, cost and reliability. The details of array technology at the die, module and board levels have been discussed in the preceding chapters. It is the purpose of this chapter to provide comparative data and some guidance in how to select a technology in consideration of the various options and strategies available based upon the application.

25.2 Dimensional-Related Advantages

Area-array interconnect results in increased I/O density throughout the packaging hierarchy. Die area, module area, board area and even cable attach area can all be reduced in size utilizing area-array components. The result can be smaller die for the same function, smaller modules for the same I/O count, smaller printed circuit boards and reduced cable connector space. This densification at all levels provides more compact and higher performing electronics with greater reliability.

25.2.1 Die I/O: Perimeter vs Area Array

Wire-bonded, perimeter-ledged chips are the most prevalent footprint and interconnect technique practiced today. One end of a wire (usually gold) is bonded to a chip I/O pad and the other end, typically about 4 mm in length, is bonded to a pad or lead frame to complete the connection from a die to the next package level. However, the number of connections is limited by the die perimeter and the density capability of the wire-bond technique. The technology limitation is anticipated to result in about a 40-μm effective off-die pitch. Increased die I/O can be achieved by using an area-array connection. Although this technique currently represents a small percentage of the chips produced, it offers a solution for higher I/O counts and high-performance requirements without
increasing die size, thereby increasing wafer productivity. In this case, the connection from a die to the next package level is usually accomplished with a solder or conductive adhesive attachment between the die and chip carrier pads to complete the connection.

The effect of I/O count on the size of both perimeter and array-leded chips is shown in Fig. 25-1. Note that the die size of chips with area-array footprints are not very sensitive to I/O count, whereas perimeter footprints can be quite sensitive to I/O count (the steeper the slope, the greater the sensitivity). For example, consider an 800-I/O application requirement. This can be achieved with a 7.5-mm die (250-μm array pitch) but requires a 16-mm die at a perimeter pitch of 75-μm, and an 11-mm die size with a 50-μm perimeter pitch. There are, however, a significant number of area-array applications in which the footprint is not fully populated. Footprints vary in population and even bump pitch to best achieve a match to chip I/O cells, chip power bussing, and to facilitate the chip-carrier design.

25.2.2 Die Support Area

The area required to provide the signal and power connections to a die can vary widely depending on the choice of connection at the die level. Table 25-1 compares the area required to connect a wire-bonded die (typically with 4.5-mm long wires) and a flip-chip die with area-array I/O. As the table shows, a 5-mm wire-bonded die consumes nearly 8X the area of a flip-chip die. Even a 15-mm perimeter-I/O die requires 2.6X more area than an area-leded die. This area difference affects not only real estate efficiency (die density) but other key aspects of electronic packages such as performance and cost discussed in later sections.

25.2.3 Relative Array Package Sizes

The most common chip-carrier for I/O counts in excess of 100 is the quad flat pack (QFP). It is inexpensive to manufacture in quantity, utilizes wire-bond interconnections between perimeter I/O die pads and a stamped lead-frame protected by an injection molded encapsulation leaving only the perimeter leads exposed. The package is limited by its poor thermal dissipation properties and the limits of perimeter I/O. Increasing the QFP size would not necessarily increase cost prohibitively but the area consumed by the package is unacceptable and ability to keep it sufficiently flat for successful assembly to a PCB is problematic. The same wire-bond process used for QFPs was adapted to connect chip I/Os to gold-plated

Table 25-1  Area requirements for area array and perimeter connected die

<table>
<thead>
<tr>
<th>Chip Size (mm)</th>
<th>Wire Bond Area</th>
<th>Flip Chip Area</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>196</td>
<td>25</td>
<td>7.8</td>
</tr>
<tr>
<td>10</td>
<td>361</td>
<td>100</td>
<td>3.6</td>
</tr>
<tr>
<td>15</td>
<td>576</td>
<td>225</td>
<td>2.6</td>
</tr>
</tbody>
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