13.1 INTRODUCTION

This chapter is a review of effective and disciplined analytical techniques which are utilized in the failure analysis of bipolar and field effect transistors (FET). Present integrated circuit complexity has increased, and device geometries have decreased to submicron dimensions. With this increase in manufacturing complexity, needs dictate state-of-the-art analytical capabilities to support product production and to continue to assure reliability. Continuous failure analysis of line and yield problems supports the refinement and achievement of a quality product. Long-term performance (field reliability) can also be improved by performing analysis on returned failed parts. Results from both analyses are continuously fed back to manufacturing and engineering for improved product quality and reliability.

Failure analysis is performed on wafers going through the line as well as finished chips placed in either hermetic or non-hermetic packages (plastic). Therefore, different techniques are required in preparing the sample for analysis. Electrical characterization is initially performed to establish if the device is operating out of specification. Once this is established, non-destructive techniques are utilized to gather the maximum amount of information. All data has to be properly documented. Then, techniques are described for opening various packages and successfully removing chips for further electrical and physical analysis.

Interconnection layers on the chip surface have increased to multi-levels (Figure 13-1). Various techniques in the preferential removal of single thin-film layers have been developed and will be explained in detail. These techniques are complemented with judicious electrical probing and isolation of the defect site causing the failure.

Once the defect is isolated, it is accessed through proper physical microsectioning techniques. In this procedure, the attributes of patience and mechanical skill of the failure analyst are tested. The defect usually is in the submicron range. It has to be observed with a...
maximum resolution instrument such as a scanning electron microscope (SEM) with field emission capabilities. This instrument can resolve structures down to the 1.0 nm range. Once the defect is resolved, photographed, and documented, additional structure exposing techniques (enhancements) such as chemical and/or plasma etching can be employed. The defect site is again photographed after structure enhancement, and usually diffusion and solid state reactions can now be observed. Other types of analysis such as microprobe, Auger and energy dispersive analysis for elemental contamination or corrosion related problems can be initially performed prior to the introduction of chemical etching. (See Chapter 14 on Analytical Methods.)

This chapter will define and explain the various procedures best suited for several incoming problems. The information covered will provide a starting point for the procedural techniques. The analyst's responsibility will be outlined as to the capabilities and limitations of several techniques. This includes definition of the problem, summarizing and verifying data, classifying accumulated data, and relating observations between the data and defined problem. A formulated hypothesis should be confirmed through the use of the available techniques. The failure analyst should thoroughly understand, and be capable of expertly coordinating all the materials, process techniques and equipment in this discipline. Ideally, the analyst should have the knowledge, judgment, initiative, and resourcefulness to use the analytical technology for effective problem-solving.

13.2 ORIGIN AND METHODOLOGY OF FAILURE ANALYSIS

13.2.1 Evolution of Failure Analysis

The origin of device failure analysis began with the invention and fabrication of the transistor. Continuous development and improvement of failure analysis techniques have followed the evolution of the semiconductor industry. Initial single transistors, such as point contact struc-
