19.1 INTRODUCTION

Burn-in has become an important tool in providing high quality electronic components to the customer. With the increasing emphasis on burn-in to improve the quality of the product, this chapter was written to provide an overview of the subject to the electronics component engineer, particularly a VLSI semiconductor engineer. Covered in this chapter is a discussion of the important parameters affecting the burn-in, how to model the effects of burn-in and how to implement an effective burn-in process.

Burn-in is a procedure that takes advantage of the nature of failures in semiconductors to improve the reliability of the product. The product is placed in a chamber that creates an environment to accelerate failure. In primitive burn-in systems, this was simply raising the temperature of the product (hence burn-in). This has evolved to systems which simultaneously raise the temperature and voltage above use conditions and apply specific functional test patterns. These stresses make failures happen faster; so that one hour of stress is equivalent to thousands or even millions of normal operating hours. Of course, burn-in could be accomplished at use conditions for a long time, but that is typically cost prohibitive.

The failures associated with VLSI product follow a curve shaped like a bathtub. (Figure 19-1). Early in life, semiconductors have a very rapidly decreasing failure rate. In the traditional view, this decreasing failure rate is followed by a constant failure rate. An alternative view (which is the one illustrated) has a failure rate which continues to decrease throughout the lifetime of the product even though it is at a much slower rate then earlier in the product's life. Under this assumption, there is no distinct center region. Finally, at the end, wear-out occurs. Wear-out induced failure is when everything begins to fail, and the failure rate increases extremely rapidly.

Burn-in works because of the shape of this curve. By accelerating the failures with burn-in,
the failure rate begins at some later time along this curve. As a result the failure rate that is shipped to a customer is reduced substantially. The amount of improvement because of burn-in depends upon how long the burn-in lasts and how much acceleration there is during the burn-in period. These effects are shown in more detail in Figure 19-2. Figure 19-2A shows the effects on the instantaneous failure rate, and Figure 19-2B shows the effects on the cumulative failure rate. The scales shown are arbitrary, but the shape is consistent with those shown previously. The displaced axis represents what happens when a burn-in of one equivalent time unit has been performed. The cumulative hazard, a method to analyze product life data, clearly shows a decrease in the number of failures that have been shipped. As the burn-in time increases, the instantaneous failure rate continues to decrease, and the burn-in becomes more effective.

It is important to be sure to avoid the wear-out region of the "bathtub" curve. If the burn-in is too long, then wear-out is brought into the normal life of the product. This is a condition to be avoided because it will lead to an insurmountable reliability problem. Another aspect to avoid is overstress. This happens when the stress conditions introduce failures that would not be seen under use conditions. If wear-out and overstress are avoided, then a well designed burn-in gives a significant improvement in the reliability. This improvement in reliability is relatively inexpensive, and with the importance of quality in the marketplace, burn-in becomes an important part of the semiconductor manufacturing process.

This burn-in chapter divides into two main areas. The first part discusses the theoretical aspects of burn-in and how to quantify the benefits and effectiveness of burn-in. This includes a review of the reliability models used today and their application to the burn-in situation. Details on the common acceleration models due to temperature, voltage and functional stress patterns are also included. Finally, the important issue of stress coverage is discussed. In many FET situations, stress coverage is the limiting factor for burn-in improvements.

The second part discusses the practical aspects of implementing a burn-in strategy. Issues related to the design of the product and of the tools important to burn-in are reviewed. This is followed by a discussion of specific issues associated with burn-in at particular levels of assembly. Burn-in is feasible at any level, from the wafer level to the final level of assembly. The chapter ends with sections on the additional benefits of burn-in and a discussion of optimizing the quality of a completed assembly, given a fixed burn-in capacity.

The bibliography at the end of the chapter is by no means complete. Instead it is intended to assist the reader in identifying additional sources of information on burn-in. Currently there are three significant overviews of the subject: Jensen and Petersen (1979), Leemis and Beneke (1990) and Kuo and Kuo (1983).

### 19.2 RELIABILITY MODELING AND FAILURES

This section describes the statistical distributions commonly used in modeling reliability.