6 Test Control Block Concepts

6.1 Introduction

The process of designing digital ICs is so complex that only by adopting a structured design methodology correct designs result within the constraints of time and financial budget. For this reason, synchronous design styles have emerged where often a distinction is made between a data path and a control path. The control path is needed to control the operation of the data path.

We have followed an identical reasoning for leaf-macro test data and test control access by considering a test data path and a test control path. We differentiate between functional paths and test paths by referring to the functional data and control path and the test data and control path. As explained in Chapter 3, the test data path may make use of the existing data path via the use of transfer properties. The transfer properties are controlled via transfer condition signals. In turn, the condition signals have to be controllable. The controllability of the transfer condition signals is handled as an item for the test data path. In cases where test data access cannot be provided via the functional data path, additional design entities are needed to enforce access. The control over these design entities is done via additional test control signals. These test control signals constitute the test control path. The combination of a leaf-macro test data path and a leaf-macro test control path is called the leaf-macro access path.

All test control signals have to be controllable during both test operation and normal operation. During test operation, the data to be applied to the test control signals has to follow the protocol stated in the leaf-macro generated test plans. During normal functional operation, the test control signals have to allow functional device operation. There are various ways to implement the test control path. For example, the functional control path can be extended, the test control signals can be connected directly to device pins, or a separate test control unit is used. To guarantee that the test control path does not interfere with the functional data and control path, and to adhere to a manageable and well defined design methodology, we have taken the approach to keep the test control path separate from the functional control path.
Normally, the test control signals are connected to additional device pins. However, the flexibility which Macro Test provides in test data path choices may lead to a complicated test control path. This may result in an unacceptable number of additional device pins. The solution to the pin count problem is to incorporate device specific test control logic in the device. This test controller is called a Test Control Block (TCB).

This chapter focuses the attention on the architecture and design of a Test Control Block. The Test Control Block is the 'conductor' of the device during test operation, whereas the functional control unit is the 'conductor' of the device during functional operation. Items to be discussed are the choice for a basic Test Control Block architecture, the Test Control Block design method, and optimization techniques to reduce the Test Control Block silicon area. Further, we shortly consider the issue of multi-layer test control. We limit our analysis to a single Test Control Block per device. At the end of this chapter, some statements are made on a multi-layer structure of Test Control Blocks.

6.2 Test Control Block Requirements

The function of a Test Control Block is to generate the required test control signal value sequences. The value sequences are defined in the leaf-macro generated test plans and may differ per design. This design dependency puts a requirement on the flexibility of a Test Control Block architecture and implementation. Further, the prime driving force for the use of a Test Control Block is limiting the number of test control device pins. Hence, a Test Control Block itself may not use too many device pins. Obviously, a Test Control Block should occupy a minimum of silicon area. Finally, the whole trajectory from Test Control Block specification to implementation should be automated and the corresponding software tools and cell library should be available in a design system as a module compiler.

6.3 Test Controller Architectures

Generation of controllers in general is a finite state machine synthesis problem. Fixed algorithms can be mapped onto a controller architecture via logic synthesis