CHAPTER 7

Applications of the SMOS Model to Digital Integrated Circuits

by Christopher J. Abel

7.1 Introduction

In this section, we will apply the statistical techniques developed in the previous chapters to two important building blocks of digital integrated circuits. First, we will examine the effect of process variations on the noise margins of a CMOS inverter, and estimate the extent to which transistor parameter variations reduce its noise immunity. We will also examine the relationship between parameter variations and the variation of the inverter delay time. The chapter concludes with an investigation of the effects of parameter mismatch on a flip-flop latch of the type used in a dynamic sense amplifier. Here, the discussion will center on the role that parameter mismatch plays in reducing the amplifier sensitivity, that is, in increasing the minimum voltage that the latch can correctly sense.

For simplicity, the analytical solutions in this chapter make use of a simplified MOS drain-current model [67-68]

\[ I_D = \beta \left( (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right) \quad (V_{GS} > V_T, \ V_{DS} < V_{GS} - V_T) \]

\[ I_D = \frac{\beta}{2} (V_{GS} - V_T)^2 \quad (V_{GS} > V_T, \ V_{DS} \geq V_{GS} - V_T) \]

\[ (7.1) \]

where \( \beta = \mu_{COX} (W/L) \). In addition, the conclusions made from this square law drain current model are supported by Monte Carlo simulations which use the SMOS model to generate statistically correct BSIM parameter decks. This guarantees the accuracy of our observations.
7.2 CMOS Inverter

7.2.1 Noise Margin

One of the primary advantages that MOS digital integrated circuits have over analog circuits is their ability to tolerate noisy input signals. For this reason, noise margin is considered to be one of the most important performance criteria of any digital circuit. Since the noise margin is a function of the MOS process parameters, random variations in the process parameters (such as $V_T$ or $\beta$) will cause variations in the noise margin. In general, the inverter is designed to have equal low and high noise margins, and variations in the parameters of the transistors in the inverter will reduce one of the noise margins and increase the other. Since the inverter is only as good as its lower noise margin, it is clear that the effect of random process variations is to reduce the inverter's noise immunity.

In this section, we will examine the effects of both interdie and intradie process parameter variation on the high and low noise margins of a CMOS inverter. After defining the low and high noise margins and relating them to the MOS process parameters $\beta$ and $V_T$, we will derive a simple analytical expression relating the statistical variances of the noise margins to the variances of $\beta$ and $V_T$. Then, the noise margin variances obtained from this expression will be compared to the more accurate variance estimates obtained from Monte Carlo simulations using the SMOS model.

We will see that both the low and high noise margins are a function of the ratio of the NMOS and PMOS mobilities, $\mu_n/\mu_p$. The effect of interdie mobility variation is reduced somewhat by the fact that the interdie mobilities have a high positive correlation. Thus, the percent variation of the ratio $\mu_n/\mu_p$ is much less than the percent variations of the individual mobilities, $\mu_n$ and $\mu_p$. The intradie variations of $\mu_n$ and $\mu_p$, however, are completely uncorrelated, and the variance of $\mu_n/\mu_p$ should be of the same order as the variances of $\mu_n$ and $\mu_p$. Thus, despite the fact that the magnitudes of the interdie parameter variations are much larger than the magnitudes of the corresponding intradie variations, we need to consider the effects of both interdie and intradie parameter variations on the noise margin.

Definition of Low and High Noise Margins

Figure 52 shows the transfer characteristic, $V_{out}$ vs. $V_{in}$, of the CMOS inverter in Figure 51, for the special case of $\beta_n = \beta_p$, where $\beta = \mu COX (W/L)$. The transfer characteristic can be divided into five separate areas [68]. Each area is characterized by one operating region (cutoff, linear, saturation) for the NMOS transistor and another for the PMOS transistor. The boundaries between the areas correspond to transitions between operating regions.

Two important points, $V_{IL}$ and $V_{IH}$, can be observed in Figure 52. $V_{IL}$ is the largest input voltage which can still be considered a logic low, while $V_{IH}$ is the smallest voltage which can still be considered a logic high.