ABSTRACT

We developed a top-down partitioning and Boolean minimization method which can be applied to fairly large combinational circuits. The method uses two-way partitioning based on ratio cut algorithm recursively. We got equivalent results for ISCAS85 circuits compared with full_simplify [9] and 20-40% reduction of literals for the largest ISCAS89 circuits within 1.5 CPU hours of SPARC2 excluding trivial redundancy, such as inverter chains.

5.1 INTRODUCTION

In the past couple of years, there has been much progress in Boolean minimizers, which utilize don’t cares sets derived from circuit structures, such as Satisfiability don’t cares and Observability don’t cares. Notions of permissible functions [1], applying Binary Decision Diagrams [8] to represent don’t care
sets [7], filtering don’t care sets [4], using image computation method for don’t care computation [9], and others including [2, 3, 5, 10, 17] enable us to apply Boolean minimizers to fairly large circuits effectively and efficiently.

However, there still remain many practical circuits which cannot be handled by Boolean minimizers. For example, there is not a little demand to minimize all combinational block of an entire chip at the same time so that we can get circuits for smaller gate arrays or standard cells. Algebraic minimizers and rule-based systems may be able to be applied to those large circuits, but their minimization quality is not good and their minimization results are greatly influenced by the quality of initial circuits, i.e., if the initial given circuit is good, then the minimization result is good, but if not, the result is not good either.

In this paper, we present a Boolean minimization method for large multi-level combinational circuits based on top-down circuit partitioning. Although Boolean minimizers has given much better performance than algebraic or rule-based methods in minimization quality, they cannot handle large circuits (e.g., circuits larger than thousands of gates) due to memory and/or computation time problems. One promising way of solving these problems is to partition a circuits into smaller ones which can be processed by Boolean minimizers. We developed a top-down circuit partitioning method using ratio cut partitioning algorithm [11, 12] so that each partitioned circuit is large enough and its internal components are connected with each other densely enough in order for Boolean minimizers to utilize don’t care sets derived from circuit structures.

There have been works on using circuit partitioning for minimizing large combinational circuits [15, 13, 14]. Although Corolla based circuit partitioning approach gives good results in terms of both circuit area and testability, it is designed mainly for technology-mapped circuits, i.e., it does not consider sizes of circuit components or it assumes that each circuit component has similar size. However, it is very effective and in some sense it is essential to apply Boolean minimizers to technology-independent circuits in order to get highly minimized circuits. In technology-independent circuits, sizes of modules in a circuit can vary very much in the sense that numbers of the literals of the largest module can be ten times or more larger than the smallest ones.

Another important point when applying partitioning for Boolean minimization is that each partitioned circuit is large enough and its internal components are connected with each other densely enough in order for Boolean minimizers to utilize don’t care sets derived from circuit structures. This means we should partition circuits into sub-circuits which are loosely coupled with each other,