Chapter 3

The CMOS Inverter

Complementing a logical variable $A$ to give $\bar{A}$ is accomplished using a basic inverter circuit. A standard CMOS inverter is quite simple and is built using two opposite-polarity MOSFETs in a complementary manner. The circuit gives a large output voltage swing and only dissipates significant power when the input is switched; these are two important properties of CMOS logic circuits. This chapter provides a detailed examination of a CMOS inverter and sets the foundations for most higher-level CMOS designs.

3.1 Circuit Operation

Figure 3.1 shows a CMOS inverter circuit. The input voltage $V_{in}$ is connected to the gate of both an nMOS and a pMOS transistor. The output voltage $V_{out}$ is taken from the common drain terminals. Transistor placement is chosen in a manner that ensures only one of the MOSFETs conducts when the input is at a stable low or high voltages. Although somewhat superfluous, we will refer to this type of transistor arrangement as fully-complementary CMOS structuring to distinguish it from other approaches to CMOS circuits.

The inverter circuit operation can be understood by examining the relationship between $V_{in}$ and the gate-source voltages of the MOSFETs. We see that

$$V_{GSn} = V_{in}$$
$$V_{SGp} = V_{DD} - V_{in},$$

where $V_{in}$ is assumed to be in the voltage range $[0, V_{DD}]$. 

J. P. Uyemura, *Circuit Design for CMOS VLSI*  
A high input voltage of $V_{in} = V_{DD}$ gives

$$V_{GSn} = V_{DD}$$
$$V_{SGp} = 0,$$  \hspace{1cm} (3.2)

so that the p-channel MOSFET $M_p$ is in cutoff while the n-channel MOSFET $M_n$ is conducting in the non-saturated mode. $M_n$ thus provides a current path to ground giving

$$\text{min}[V_{out}] = V_{OL} \approx 0.$$  \hspace{1cm} (3.3)

Conversely, a low input voltage of $V_{in} = 0$ results in

$$V_{GSn} = 0$$
$$V_{SGp} = V_{DD}$$  \hspace{1cm} (3.4)

which shows that $M_n$ is in cutoff, while $M_p$ conducts in the non-saturated mode. The pMOS transistor $M_p$ then provides a path to the power supply so that

$$\text{max}[V_{out}] = V_{OH} \approx V_{DD}.$$  \hspace{1cm} (3.5)

Because of the placement and operation of each MOSFET, $M_n$ is often called a pull-down transistor, while $M_p$ is termed a pull-up device.

The DC input-output characteristics are portrayed graphically using the Voltage-Transfer Curve (VTC) shown in Figure 3.2. This is simply a plot of $V_{out}$ as a function of $V_{in}$. The inversion operation is seen directly from the curve: when $V_{in}$ is small, $V_{out}$ is large, and vice-versa\(^1\). Qualitatively, the sharpness of the transition is a measure how well the circuit is

![Figure 3.1: CMOS Inverter](image)

\(^1\)Qualitatively, the sharpness of the transition is a measure how well the circuit is