Abstract: With reference to the mainstream technology, the most relevant failure mechanisms which affect yield and reliability of Flash memory are reviewed, showing the primary role played by tunnel oxide defects. The effectiveness of a good test methodology combined with a proper product design for screening at wafer sort latent defects of tunnel oxide is highlighted as key factors for improving Flash memory reliability. The degradation of device performance induced by program/erase cycling is discussed, covering the behavior of a typical cell, the evolution of memory array distribution, and the single bit failure modes. Oxide traps are demonstrated to be responsible for the most critical failure mechanisms, like the erratic erase and the single bit data loss: the impact of stress-induced leakage current on data retention is shown to limit the scalability of tunnel oxide thickness. Finally, reliability implications of multilevel cell concept are briefly analyzed.

7.1 INTRODUCTION

Flash memory has become in the most recent years the star among non volatile memories because it offers the capability of being electrically erased and rewritten, so far featured only by the expensive EEPROM’s, at a cost comparable to the one of EPROM’s.

Together with the desirable features which make it so attractive, Flash memory unfortunately combines also the yield and reliability issues of EPROM’s and EEPROM’s (Fig. 7.1), plus some additional ones which are specific of this technology. Writing operations involve both Fowler-Nordheim tunneling and hot
carriers; program/erase cycling endurance must be achieved without degrading data retention; the single transistor structure exposes memory cells to array disturbs and to over-erasure problems.

All these issues make the Flash technology one of the most difficult to be mastered, requiring a very accurate process optimization and a severe process control [1].

The single most important factor contributing to yield and reliability of Flash memory is the quality of tunnel oxide, both in terms of intrinsic properties and defect density.

Uniformity of tunnel current, which determines the width of the erased $V_t$ distribution within a memory array, and oxide wear-out under current stress, which affects memory endurance, are much related to tunnel oxide process conditions. Point defects which cause a local increase of tunnel oxide conductivity are responsible for single bit over-erasure and single bit failures due to program disturb, the most relevant yield problems in Flash memories.

Major efforts have been devoted in the last few years to improve the way of evaluating and monitoring the quality of tunnel oxide, for what concerns both electrical test methodology and the related test structures [2–4].

Moreover, the high degree of testability of Flash memories allows to screen at wafer sorting latent defects which may cause single bit failures related to program disturbs, data retention and premature oxide breakdown.

With reference to the mainstream technology, this chapter will review the major issues impacting yield and reliability of Flash memory, it will discuss in