Chapter 6

Parameter extraction of lightly-doped drain (LDD) MOSFETs

Modern MOSFETs often incorporate a lightly-doped drain (LDD) region. Due to the presence of the LDD region, these so called LDD MOSFETs have a smaller electric field near the drain region and therefore a reduced hot-carrier effect over the conventional MOSFET [1-2]. This, however, comes with the expenses of an increase in the drain/source series resistances and therefore a reduced drain current level. Figures. 6.1(a)-(c) give the schematic of the cross section of conventional MOSFET, LDD MOSFET, and fully overlapped LDD (FOLD) MOSFET, respectively. It can be seen that the LDD and FOLD MOSFETs differ mainly in the gate structure; the LDD MOSFET has a typical polysilicon gate surrounded by the oxide sidewall, whereas the FOLD MOSFET has a larger gate consisting of a polysilicon gate and two spacers. Let us focus on the LDD MOSFET. The lightly and heavily doped drain and source regions are fabricated as follows. First, the lightly-doped n⁻ drain and source regions are formed by ion implantation defined by the edges of the polysilicon gate. The heavily-doped n⁺ drain and source regions are then formed by a second ion implantation defined by the edges of the oxide sidewalls.

Because the free-carrier density in the portion of the n⁻ drain and source regions underneath the gate can be easily modulated by the gate bias, the drain and source series resistances and the effective channel length of the LDD device become gate-voltage dependent. This, when using the Terada-Muta method [3] developed intended for the conventional MOSFET to extract the LDD parameters, may result in a situation where no unique intersection can be found in the total resistance versus mask channel length plot, as shown in Fig. 6.2.

In this chapter, we will first investigate the validity of the Terada-Muta method for extracting the effective channel length $L_{\text{eff}}$ of the LDD MOSFET. A measurement algorithm to extract the bias-dependent effective channel length and drain and source series resistance of LDD MOSFET is then discussed. Another $L_{\text{eff}}$ extraction method which proposed a different concept that the effective channel length of the LDD MOSFET should be bias independent is also presented.
Extraction of other parameters of the LDD MOSFET, such as the drain and source resistances, metallurgical channel length, and threshold voltage, will also be addressed. Both measurement data and device simulation results will be used to facilitate and demonstrate the extraction process.

Figure 6.1: Schematic of the (a) conventional MOSFET, (b) LDD MOSFET, and (c) fully overlapped LDD MOSFET (after Takeuchi et al. [10]).