6 CIRCUIT IMPLEMENTATION OF DELTA-SIGMA MODULATORS

6.1 INTRODUCTION

In this chapter, we discuss the implementation details of delta-sigma modulators. Our primary target applications are data acquisition and low frequency instrumentation. Therefore, the extremely high linearity is our top design priority. A complete second order delta-sigma modulator has been fabricated and the nonlinearity results were reported in Chapter 4. However, copyright issues prevent us from discussing the implementation details. As an integral part of our research, instead, we examine the design issues for a first order delta-sigma modulator. This chapter is arranged as follows. Section 6.2 outlines the overall structure for a first order delta-sigma modulator and its timing diagram. Section 6.3 discusses the design of the integrator. The need for auto-zeroing technique is addressed and the principle of one implementation is explained. Section 6.4 is devoted to the design of the opamp. The optimal design principle and design strategy developed in the previous chapters are applied here to determine the supply current and device sizes. The fully differential implementation of the integrator requires a common mode feedback (CMFB) circuitry to stabilize the common mode output voltage of the fully differential opamp. The
In this section, the system level diagram of a first order delta-sigma modulator is presented. The building block designs are discussed in detail in the following sections. The whole system is implemented using fully differential circuit, and a two-phase nonoverlapping clocking scheme is employed. The overall block diagram is shown in Figure 6.1. A first order delta-sigma modulator consists of four main building blocks: the fully differential integrator, the comparator, the D-latch and the digital control circuitry. The switch control signals that are associated with each building block are also shown in Figure 6.1. The cross sampling block is actually the sampling stage (input stage) of the integrator. We deliberately separate them out from the integrator in order to emphasize the nature of the sampling, which will be explained in detail in Section 6.3. The letter "d" and "dd" that appear in the subscript of clocking signals $\Phi_1$ and $\Phi_2$ stand for delayed versions of the corresponding phases. For example, the clocking signal $\Phi_{1d}$ stands for the delayed version of $\Phi_1$, and $\Phi_{1dd}$ the delayed version of $\Phi_{1d}$. The timing diagram for all the phases are depicted in Figure 6.2. Text that appears to the left of the each phase shows which building block is controlled by that signal. A brief description for each phase