2 Analog Phase-Locked Loops

2.1 Time Domain Analysis of Phase-Locked Loops

A complete Phase-Locked Loop (PLL) block diagram is shown in Figure 2.1. The PLL is receiving a signal s(t), which has an unknown phase, \( \theta(t) \) to the receiver. Viterbi [18] has described the phase-locked loop as a communications receiver that adjusts the local oscillator frequency and phase according to its measured phase error. Although PLLs are found in applications besides receivers, the PLL in Figure 2.1 is performing as a local oscillator to coherently demodulate the received signal. (Recall from communication theory that coherent demodulation provides a 3 dB improvement in signal-to-noise. In Chapter 11 we will show that the signal-to-noise improvement is 6 dB inside a synchronization loop.)

In Figure 2.1, we assign an amplitude, \( \sqrt{2P} \), to the received signal, s(t), where P is the power in the signal. Initially, the magnitude \( \sqrt{2P} \) for the received signal may seem awkward. Recall however, the power in the signal \( x(t) = A \cos(2\pi ft) \) is \( P = A^2/2 \). Algebraic manipulation yields \( A = \sqrt{2P} \), the assumed magnitude for the input phasor in Figure 2.1. In some applications such as frequency synthesizers, the signal into the phase-locked loop has a fixed signal level and a high Signal-to-Noise Ratio (SNR). More stressful on loop performance however, are those applications with varying signal levels and low SNRs. In our subsequent derivations we will see that these two parameters affect the performance of the loop.
The phase detector for a PLL measures the phase difference between the input signal and the PLL’s voltage controlled oscillator. This phase difference is converted to a voltage in the phase detector, which is then used to provide feedback control to the local oscillator. Associated with the phase detector is a gain, $K_{detector} = K_d$, which represents the mapping of the phase error in radians to an output with units, volts/radians. In Figure 2.1, the phase detector is represented as a mixer with a lowpass filter, which is a common implementation. An ideal mixer will produce a frequency difference component and frequency summation component,

$$\cos(2\pi f_0 t + \theta) \cdot \sin(2\pi f_0 t + \dot{\theta})$$

$$= \frac{1}{2} \sin[4\pi f_0 t + \theta + \dot{\theta}] + \frac{1}{2} \sin[\theta - \dot{\theta}]$$

where

$\theta$ is the signal's unknown phase

$\dot{\theta}$ is the PLL's estimate of the phase, $\theta$

In analog phase-locked loops, we are most interested in the baseband component, $\frac{1}{2} \sin[\theta - \dot{\theta}]$ that is used to generate an error voltage for