In the previous chapters, we have discussed methods to reduce power consumption at various levels of design abstraction. The methods are general-purpose because they can be applied to wide varieties of circuits. We have focused on the general techniques of low power design with some specific examples to highlight their applications. In this chapter, we will present some special low power techniques that can be applied to certain types of circuits. The special techniques typically exploit certain unique properties of the circuit and often results in dramatic power reduction.

There is no clear distinction between “general” and “special” techniques. The difference is in the scope of their applications. The special techniques require more manual effort because design automation in these areas is less mature. Although the techniques are termed “special,” their applications could be very important because the circuits are used in many VLSI chips; for example, the low power clock, bus and SRAM techniques. Despite the narrow scope of application, it is hoped that the techniques featured in this chapter could become a source of inspiration for the readers.

6.1 Power Reduction in Clock Networks

In a synchronous digital chip, the clock signal is generally one with the highest frequency. The clock signal typically drives a large load because it has to reach many sequential elements distributed throughout the chip. Therefore, clock signals have
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been a notorious source of power dissipation because of high frequency and load. It has been observed that clock distribution can take up to 40% of the total power dissipation of a high performance microprocessor [6.1]. Furthermore, the clock signal carries no information contents because it is predictable. It does not perform useful computation and only serves the purpose of synchronization. The number of different clock signals on a chip is very limited and warrant special attention during the design process. As such, many special techniques have been devoted to the power efficiency of clock generation and distribution.

6.1.1 Clock Gating

In Section 5.2, we discussed signal gating as a general means to mask unwanted signal transitions from propagating forward. The same idea has been applied to clock signals.

Clock gating, as depicted in Figure 6.1, is the most popular method for power reduction of clock signals. When the clock signal of a functional module (ALUs, memories, FPUs, etc.) is not required for some extended period, we use a gating function (typically NAND or NOR gate) to turn off the clock feeding the module. Note that the gating signal should be enabled and disabled at a much slower rate compared to the clock frequency. Otherwise the power required to drive the enable signal may outweigh the power saving. Clock gating saves power by reducing unnecessary clock activities inside the gated module.

![FIGURE 6.1 Clock gating.](image)

Clock gating has been successfully used in recent high performance CPU designs [6.2]. One reason is that in a CPU chip, some functional modules may be left idle for an extensive period depending on the software it is executing, for example the floating point unit of a CPU. The design complexity and performance degradation of clock gating are generally manageable. The gated clock signal suffers an additional gate