TEST METHODS FOR WAFER-SCALE INTEGRATION

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INTRODUCTION

Wafer-scale integration (WSI) is expected to yield higher speed and better reliability and to drastically improve circuit density. The essential problem is that WSI cannot be fabricated without defects because the number of defects increases with circuit area. WSI systems require redundant silicon areas to enhance yield, and must be reconfigured by detecting faulty parts and substituting them with spares. It is important to obtain adequate yield by decreasing the redundant area as much as possible.

WSI testing is also a severe problem because of redundancy and increasing complexity of circuits. WSI testing presents three problems: (1) Test costs are high because a very large number of subsystems must be tested, and then the WSI system formed by connecting the good subsystems must itself be tested. (2) Inner nodes are difficult to observe because the pad-to-gate ratio is very low and a WSI system does not have enough external test pads for large circuits to be tested. (3) Conventional VLSI testers cannot be used, thus special test equipment is required. The optimum solution to these problems would be to build self-diagnostic facilities into the WSI system itself.

This paper discusses WSI test methods. First we present a survey of WSI test methods which have been studied so far, and discuss the implementation of a built-in self-test (BIST) technique to the wafer-scale fast Fourier transform (FFT) processor, and then discuss WSI fabrication.

WSI TEST METHODS

Conventional probe tests should be used for final WSI system test because it is necessary to indicate that the power can be supplied to the system from external I/O pads and the system can be correctly operated before assembly. Since there are not enough external I/O pads to test the inner circuits due to test cost, area overhead, and test equipment, this method should be used in combination with the test methods described below.
A test method using laser cutting and linking has been reported. The structure for a laser link is a sandwich of amorphous silicon between two metal layers. Laser links are made as follows: The second metal, an amorphous silicon, and part of the first metal melted by the laser spot create a silicon-aluminium alloy. Metal is also cut by laser. The connection paths for testing subsystem can be made and tested. After routing the entire WSI system, the connection paths for testing can be created and are cut after testing. Laser cutting and linking can be done at the end of manufacturing. The area overhead of linking and cutting points is required and this method cannot be performed repeatedly at the same point.

Test methods using MNOS (metal-nitride-oxide semiconductor) transistors have also been studied. The MNOS transistors used as electrically programmed nonvolatile switches have a structure such that the usual gate oxide layer in a MOS (metal-oxide semiconductor) transistor is replaced by a silicon nitride layer over silicon dioxide. The high voltage applied to the gate electrode causes the thin silicon dioxide layer to become conductive. The signal paths for testing subsystem can be thus formed. The MNOS transistors can be repeatedly programmed without significant damages. The area overhead of transistor switches, MNOS transistors and interconnects to external pads to control MNOS transistors is required.

Test methods using floating gate FETs programmed by electron beam (EB) have been reported. A floating gate FET has a completely oxide-encapsulated polysilicon gate. Electrons are injected by the EB into the oxide overlying the gate and the charge is trapped on the floating gates. The floating gate FET turns off if an EB applied to the gate. The charge can be erased with an ultraviolet light exposure. This mechanism is reliable and is commonly used in erasable programmable read only memories (EPROMs). The signal paths for testing subsystems can be formed. The floating gate FETs can be programmed repeatedly. The area overhead of floating gate FETs is required.

Test methods using logical circuits have been studied. Electrical logical switches are used to test subsystems and to configure the WSI system composed of these working subsystems. The connection and test of configuration logic are first performed, and each subsystem is tested. Thus the WSI system is formed by serially connecting subsystems with external software control. This method provides repeated and dynamic testing. The area overhead of configuration logic is required. The problem with this method is that the system cannot be formed if the configuration logic suffers a power-short failure.

Testable design utilizing the regularity of WSI systems, for example the systolic array, has been reported. Test vectors enter from one side of the array and identical results from some signal paths are compared taking into account delay time at the other side of the array. This method strongly depends on the system architecture.

The BIST technique for WSI has also been proposed. This method generates the test vectors and compares the result. The on-chip hardware to perform the BIST is provided in the circuit itself, and circuits are partitioned into a number of testable units, for example combinational logic units. Although overhead costs for BIST circuitry is required and testing time is longer, the BIST has the advantages described below. The inner subsystems can be tested by a small number of external I/O pads. The hierarchical test, for example PE test and entire WSI system test, can be performed. No new process technology and special test equipment are required. It is not necessary to generate test vectors. Thus the BIST