6

OFF-LINE QUALITY CONTROL IN INTEGRATED CIRCUIT FABRICATION USING EXPERIMENTAL DESIGN

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6.1 INTRODUCTION AND SUMMARY

This paper describes and illustrates the off-line quality control method, which is a systematic method of optimizing a production process. It also documents our efforts to optimize the process for forming contact windows in 3.5-μm technology complementary metal-oxide semiconductor (CMOS) circuits fabricated in the Murray Hill Integrated Circuit Design Capability Laboratory (MH ICDCL). Here, by optimization we mean minimizing the process variance while keeping the process mean on target.

A typical very large scale integrated circuit (IC) chip has thousands of contact windows (e.g., a BELLMAC\textsuperscript{1} -32 microprocessor chip has 250,000 windows on an approximately 1.5-cm\textsuperscript{2} area), most of which are not redundant. It is critically important to produce windows of size very near the target dimension. (In this paper windows mean contact windows.) Windows that are not open or are too small result in loss of contact to the devices, while excessively large windows lead to shorted device features. The application of the off-line quality control method has reduced the variance of the window size by a factor of four. Also, it has substantially reduced the processing time required for the window-forming step.

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This study was inspired by Professor Genichi Taguchi’s visit to the Quality Theory and Systems Group in the Quality Assurance Center at Bell Laboratories during the months of August, September, and October, 1980. Professor Taguchi, director of the Japanese Academy of Quality and a recipient of the Deming award, has developed the method of off-line quality control during the last three decades. It is used routinely by many leading Japanese industries to produce high-quality products at low cost. An overview of Professor Taguchi’s off-line and on-line quality control methods is given in Taguchi\cite{1} and Kackar and Phadke.\cite{2} This paper documents the results of the first application of Professor Taguchi’s off-line quality control method in Bell Laboratories.

The distinctive features of the off-line quality control method are experimental design using orthogonal arrays and the analysis of signal-to-noise ratios (s/n). The orthogonal array designs provide an economical way of simultaneously studying the effects of many production factors\cite{2} on the process mean and variance. Orthogonal array designs are fractional factorial designs with the orthogonality property defined in Section 6.4. The s/n is a measure of the process variability. According to Professor Taguchi,\cite{3} by optimizing the process with respect to the s/n, we ensure that the resulting optimum process conditions are robust or stable, meaning that they have the minimum process variation.

The outline of this paper is as follows: Section 6.2 gives a brief description of the window-forming process, which is a critical step in IC fabrication. The window-forming process is generally considered to be one of the most difficult steps in terms of reproducing and obtaining uniform-size windows. Nine key process factors were identified and their potential operating levels were determined. A description of the factors and their levels is given in Section 6.3. The total number of possible factor-level combinations is about six thousand.

The aim of the off-line quality control method is to determine a factor-level combination that gives the least variance for the window size while keeping the mean on target. To determine such a factor-level combination we performed eighteen experiments using the $L_{18}$ orthogonal array. The experimental setup is given in Section 6.4. These eighteen experiments correspond to eighteen factor-level combinations among the possible six thousand combinations. For each experiment, measurements were taken on the line width and the window-size control features. The resulting data were analyzed to determine the optimum factor-level combination. The measurements and the data analysis are presented in Sections 6.5 through 6.9.

The optimum factor levels, inferred from the data analysis, were subsequently used in fabricating the BELLMAC-32 microprocessor, the BELLMAC-4